CRYSTALLINE SILICON SURFACE PASSIVATION BY HYDROGENATED AMORPHOUS SILICON LAYERS DEPOSITED BY HWCVD, RF PECVD AND VHF PECVD: THE INFLUENCE OF THERMAL ANNEALING ON MINORITY CARRIER LIFETIME

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ABSTRACT: In this work we report on the influence of thermal annealing on the average minority carrier lifetime of c-Si wafers which are passivated on both sides by intrinsic a-Si:H layers with a thickness of 50 nm made by different deposition techniques. We found that for a-Si:H layers deposited at a low temperature (T < 130°C) and annealed at a higher temperature (T = 200°C), this influence is particularly strong; typically leading to an increase in minority carrier lifetimes of two orders of magnitude after prolonged annealing. This behavior is observed for RF PECVD, VHF PECVD as well as for HWCVD. For all deposition methods we have obtained minority carrier lifetimes of approximately 4 ms at a minority carrier density of 10^{15} cm^{-3} and the lifetime characteristics as a function of annealing time are highly similar. We have also fabricated a sample by HWCVD at a relatively high temperature of 250°C, which has an as-deposited minority carrier lifetime at 10^{15} cm^{-3} of 2.0 ms, higher than for the as-deposited layers at low temperature, which however stayed roughly constant upon prolonged annealing at 200°C. Our results indicate that prolonged thermal annealing has a strong effect on the passivation quality, provided that the a-Si:H layers are deposited at low temperatures, and that this effect occurs regardless of the deposition method. Moreover, our results indicate that the deposition temperature is a more critical parameter for the annealing characteristics and the final minority carrier lifetime than the deposition method is.
Keywords: Heterojunction, Passivation, Annealing

1 INTRODUCTION

Surface passivation of the a-Si:H/c-Si interface is a key feature in optimizing the performance of silicon heterojunction (SHJ) solar cells. To obtain open circuit voltage (V_{OC}) values exceeding 700 mV for such cells, excellent surface passivation is required. Sanyo [1] has first introduced the concept of depositing a thin intrinsic layer of a-Si:H between the base and the emitter of SHJ solar cells. With this method, they have recently achieved an efficiency of 23% and a V_{OC} of 729 mV [2]. These outstanding results have inspired many other groups around the world to focus on the fabrication of SHJ cells and to investigate the passivation properties of intrinsic a-Si:H layers on c-Si.

De Wolf [3] *et al* have shown that long term annealing has a great influence on the minority carrier lifetime of c-Si wafers, which are passivated by intrinsic hydrogenated amorphous silicon (a-Si:H) layers deposited at relatively low (130-180°C) substrate temperatures. For passivation samples, consisting of c-Si wafers with at both sides a 50 nm intrinsic a-Si:H layer, deposited at 130°C by VHF PECVD, they have measured a minority carrier lifetime of only 12.2 µs directly after deposition. After annealing at T = 180°C, however, this lifetime showed a drastic increase; after 1 h of annealing, this lifetime was already higher than 500 µs. Prolonged annealing led to much higher lifetimes, saturating at 4.4 ms.

Inspired by this work, we investigated this phenomenon for our passivation layers. In this study, however, we compared a-Si:H layers fabricated by three different deposition methods, i.e. standard RF PECVD, VHF PECVD and HWCVD. We have the unique advantage in our lab that we can deposit optimized thin intrinsic a-Si:H layers by these three different deposition methods. Comparing these different fabrication methods is of interest since the reduced ion bomardment in VHF PECVD and especially in HWCVD compared to standard RF PECVD [4] could be advantageous for the quality of c-Si surface passivation [5]. High energy ion bombardment is expected to lead to enhanced damage and defect creation in c-Si wafers [5,6]. In this work we show high quality c-Si surface passivation by a-Si:H fabricated at low temperatures by these three methods: RF PECVD, VHF PECVD, and HWCVD, and show the differences in passivation quality versus anneal time. For comparison, we have also fabricated a HWCVD sample at a higher temperature (T = 250°C).

2 EXPERIMENTAL

In this research, we have used n-type 2-5 Ωcm double sided polished <100> FZ c-Si wafers with a thickness of approximately 280 µm. Prior to a-Si:H deposition, these wafers were dipped in HF (1% diluted in H_2O) for 2 minutes. Next, approximately 50 nm thick a-Si:H layers were deposited on both sides of the c-Si wafer. Between these two depositions, the wafers had to be flipped in air, without performing an additional HF dip. The RF PECVD depositions were performed in our PILOT system [7] at a power density of 30 mW/cm^2, a pressure of 0.5 mbar and a temperature of 125˚C, using pure SiH_4. These conditions led to a deposition rate of 0.15 nm/s. The VHF PECVD depositions have been performed in our ASTER system [8] at a power density of 31 mW/cm^2, a pressure of 0.16 mbar and a temperature of 130˚C, using SiH_4 and H_2 as source gases at a flow ratio of 1:1,

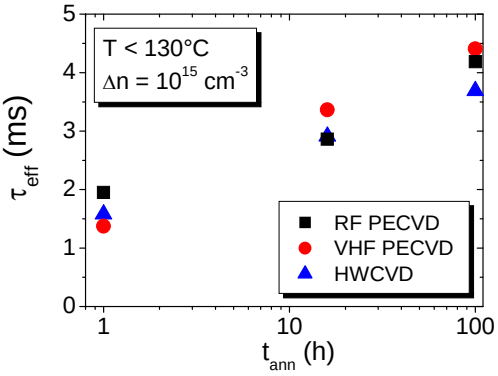

Figure 1, Minority carrier lifetimes at an injection level of 10^{15} cm^{-3} plotted against anneal time for the three different deposition methods.

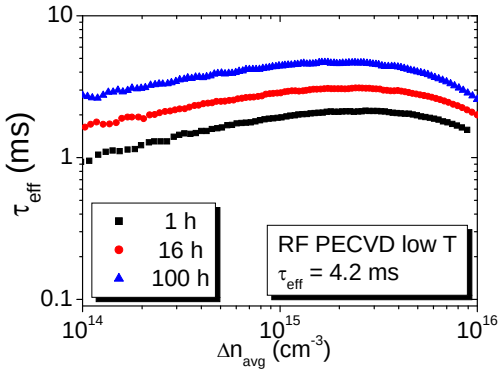

Figure 2, Injection level dependent minority carrier lifetimes of the sample deposited by RF PECVD after 1 h, 16 h and 100 h of thermal annealing at 200°C in N_2.

leading to a deposition rate of 0.28 nm/s. The HWCVD depositions have been performed in our PASTA system [9], using pure SiH_4 at a pressure of 0.005 mbar and a wire temperature of 1820°C, leading to a substrate temperature of 130°C. The substrate temperature was achieved by radiation from the resistively heated filaments only. The deposition rate was equal to 0.03 nm/s. More details about the used reactor can be found elsewhere [10]. The high temperature HWCVD sample was deposited in the PILOT system, which can be operated in a continuous in-line HWCVD mode [11]. The substrate temperature of 250°C was reached due to radiation from the resistively heated wires only. The wires were heated at a temperature of 1890°C. Pure SiH_4 was used for the fabrication of this sample at a pressure of 0.025 mbar. The 50 nm thick a-Si:H layers were fabricated using a linear speed of 80 mm/min in the continuous in-line HWCVD mode, which roughly corresponds to 1 nm/s under comparable stationary deposition conditions [11]. This deposition rate is considerably higher than the rates for all low T passivation samples, especially the HWCVD sample. A high deposition rate (1-3 nm/s) has been shown to be crucial to obtain excellent surface passivation for a-Si:H layers deposited by ETP [12] at temperatures above 350°C on similar c-Si wafers used in this work since such higher deposition rates prevent epitaxial growth [13]. For the deposition methods used in this work (RF PECVD, VHF PECVD, and HWCVD), increasing the deposition rate might also be useful to prevent epitaxial growth when increasing the deposition temperature.

After deposition, all samples were annealed at 200°C in N_2 ambient for various anneal times; 1 h, 16 h and 100 h, respectively.

Table 1, Minority carrier lifetimes at an injection level of 10^{15} cm^{-3} for all samples after different anneal times.

t_{ann} (h)	RF PECVD τ_{eff} (ms)	VHF PECVD τ_{eff} (ms)	HWCVD low T τ_{eff} (ms)	HWCVD high T τ_{eff} (ms)
0	1.5 10^{-2}	4.4 10^{-2}	8.7 10^{-2}	2.0
1	1.9	1.4	1.6	2.2
16	2.9	3.4	2.9	2.3
100	4.2	4.4	3.7	2.3

The lifetime of the samples was measured by means of the Quasi Steady State Photoconductance (QSSPC) method [14], using the so-called quasi transient mode and the generalized mode [15].

3 RESULTS AND DISCUSSION

Directly after deposition, the sample for which the surface passivating intrinsic a-Si:H layers were deposited by RF PECVD showed a minority carrier lifetime at an injection level of 10^{15} cm^{-3} of only 15 µs, similar to [3]. The sample for which the intrinsic a-Si:H layers were deposited by VHF PECVD showed a minority carrier lifetime of 44 µs and the sample for which these layers were made by HWCVD showed an as-deposited minority carrier lifetime of 87 µs. The high temperature HWCVD sample immediately showed a device quality as-deposited minority carrier lifetime of 2.0 ms at the same injection level (see Table1).

In Figure 1, the minority carrier lifetimes of the different low T samples at an injection level of 10^{15} cm^{-3} are shown versus the anneal time. In Figure 2, the injection level dependent minority carrier lifetime is shown for the low T RF PECVD sample. As can be seen from Figures 1 and 2 and Table 1, prolonged annealing leads to greatly enhanced minority carrier lifetimes for all low T samples. As can be seen from Figure 2, the increase in lifetime is similar throughout the whole measured range of injection levels. The characteristics are similar for all deposition methods at low T.

After 100 h of annealing, all three samples show an excellent minority carrier lifetime around 4 ms at an injection level of 10^{15} cm^{-3}.

In addition to the samples described above, we have also fabricated a HWCVD sample at a relatively high substrate temperature of 250°C. The injection level dependent annealing characteristics of the HW samples are shown in Figure 3. In Figure 4, the characteristics of the low T and high T HWCVD samples at an injection level of 10^{15} cm^{-3} are shown in the same plot. For the high T sample (see Figure 3 and 4, and Table 1), the

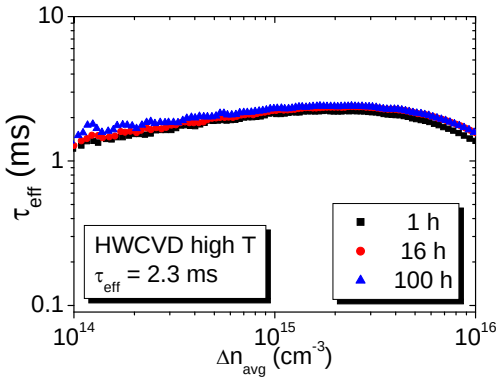

Figure 3, Injection level dependent minority carrier lifetime of a HWCVD sample deposited at 250°C after 1h, 16 h and 100 h of annealing in N_2.

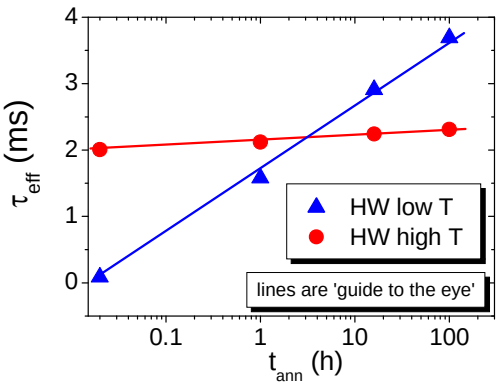

Figure 4, Annealing characteristics for low T (120°C) and high T (250°C) passivation samples made by HWCVD. The lines are a guide to the eye.

minority carrier lifetime stays roughly constant upon prolonged thermal annealing.

From the results shown in Figures 1-4 and Table 1 we conclude that the deposition temperature is a more important parameter than the method of deposition. Since the deposition method does not seem to have a significant influence on the annealing characteristics, we conclude that the impact of ion bombardment on the annealing characteristics and passivation properties of our samples is not very crucial for the presently used deposition parameters.

The effect of the deposition temperature, on the other hand, is very pronounced. Lowering the deposition temperature typically leads to an increased amount of hydrogen that is bonded as multihydrides ($Si\text{-}H_{n>1}$) for **AS-DEPOSITED** a-Si:H layers [3]. The presence of higher hydrides has a detrimental effect on the minority carrier lifetime [16]. This effect has been observed to be stronger if these multi-hydrides are present close to the a-Si:H/c-Si interface, and less detrimental if they occur in the a-Si:H layers away from the a-Si:H/c-Si interface [17]. Prolonged annealing is expected to lead to a bonding rearrangement of the hydrogen in a-Si:H, which will lead to a relatively higher Si-H versus $Si\text{-}H_{n>1}$ bond density and therefore a strongly enhanced minority carrier lifetime [3].

Furthermore, increasing the deposition temperature typically leads to an increased crystalline fraction in the deposited layers [18]. An increased crystalline fraction in the layers also leads to a decrease in passivation improvement upon annealing [18,19]. Spectroscopic ellipsometry measurements performed on our high T HWCVD passivation sample indeed show a significant, yet not detrimental, crystalline fraction in the film, contrary to the samples for which the films were deposited at low T, which is in agreement with our findings.

Our results might have strong implications for device processing and manufacturing conditions of silicon heterojunction solar cells. Depositing the a-Si:H films at a higher temperature can increase the manufacturing throughput, but on the other hand enhances the risk of epitaxial growth [20]. Fabricating the samples at a lower deposition temperature and thereafter anneal them at a higher temperature might therefore be considered as a serious alternative. Increasing the deposition rate for samples that are fabricated at higher temperatures could prevent epitaxial growth as well [13].

4 CONCLUSIONS

We have obtained high quality c-Si surface passivation by a-Si:H layers deposited by three different deposition methods; RF PECVD, VHF PECVD and HWCVD. We have shown that prolonged thermal annealing can strongly increase the minority carrier lifetime of c-Si wafers passivated on both sides by intrinsic a-Si:H layers, especially when the a-Si:H layers are deposited at a relatively low temperature (T < 130°C). We have observed this effect for all studied deposition methods. This suggests that ion bombardment only plays a minor role in changing the annealing characteristics of such samples. Furthermore we have observed that a HWCVD sample which was made at a higher temperature (T = 250°C) showed good as-deposited passivation, but did not show significant passivation improvement upon prolonged annealing, which is probably due to the significant crystalline fraction in the a-Si:H films, as observed by spectroscopic ellipsometry. Finally, our low T passivation samples show a higher minority carrier lifetime at the shown injection levels after prolonged annealing compared to the high T samples, which could have strong implications for device processing conditions of silicon heterojunction solar cells.

5 ACKNOWLEDGEMENTS

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