Front-end modules for ALICE SSD

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Abstract

The Silicon Strip Detector (SSD) front-end module will populate the two outer layers of the ALICE inner tracker.

After years of design and developments reported in the previous proceedings of the LECC workshop [1], [2], [3], several working prototypes of this module have been produced with the final components in two different laboratories. The first test results will be presented.

I. Introduction

In the ALICE experiment, the Inner Tracker System (ITS) makes use of SSD modules for its two external detection layers. These layers are shaped as two concentric barrels having an approximate length of one meter and a radius of 334 mm and 384 mm respectively. A total of 1698 modules is needed for the two layers. With the spares and some contingency, this leads to a production goal approaching 2000 modules representing about 3 million analogue channels and about 6 m^2 of sensors, which is the largest double-sided silicon detection surface ever used.

II. Module

The ALICE front-end module consists of a sensor, an AC coupled Double Sided Silicon Strip Detector (DSSSD), and the corresponding Front End Electronics assembly (FEE) built around the HAL25 front-end chip.

Two kapton/aluminum hybrids supporting the FEE provide a good radiation length whereas Tape Automated Bonding (TAB) using kapton/aluminum microcables connects sensor, FE chips and hybrids without using any wire bonding. These flexible connections allow folding the FEE over the sensor, providing a compact detection module and the decoupling of the geometrical position from the liquid cooling means. Figure 1 shows one of these modules in an unfolded position, with the sensor in the middle and with the top hybrid connected to the upper side of the sensor and the bottom hybrid connected to the hidden side of the sensor. One can notice the flexible so-called chip-cables connecting sensor and FEE.

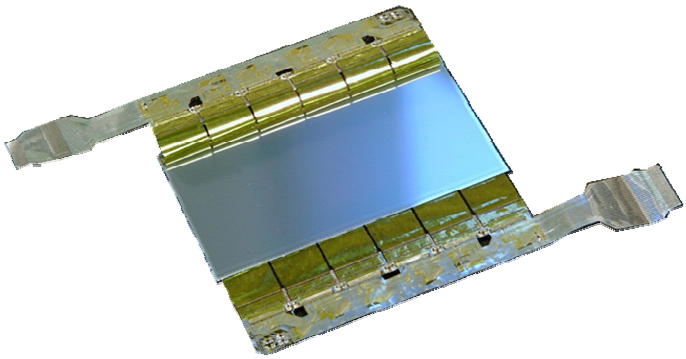

Figure 1: The front-end module with the top and bottom hybrid connecting both sides of the sensor.

III. COMPONENTS

Realistic prototypes had to be produced with real final components. Providing these components was the main task during 2002.

A. Sensor

Each sensor has a size of 75x42x0.3 mm with 768 strips on each side with a pitch of 95 µm tilted with respect to the small axis by 7.5 mrad on P-side and 27.5 mrad on N-side, forming a stereo angle of 35 mrad between strips lying on opposite faces [4].

Double sided sensors are extremely sensitive components that have to be produced on a large scale. For this reason, the production has been shared between three different providers for safety. To qualify the sensor design, 20 pre-series samples were provided by each of the three manufacturers. The production is going on allowing prototyping of more than 100 modules in the late 2002 and 2003. Measurements of the sensors will be made in two laboratories equipped with probe stations.

B. Front-end chips

The HAL25 front-end chip presented in figure 2 is the only active component on the front-end module. Designed in 0,25 µm technology it is RadTol. It includes 128 analogue channels providing a dynamic range of ±300 000 electrons (about ±14 MIPS) with an ENC of 215 e^- +25 e^-/pF. All the analogue and digital functionalities are remotely controlled by JTAG protocol. Chip shape, and also input and output pitch have been optimized for TAB bonding [5], [6].

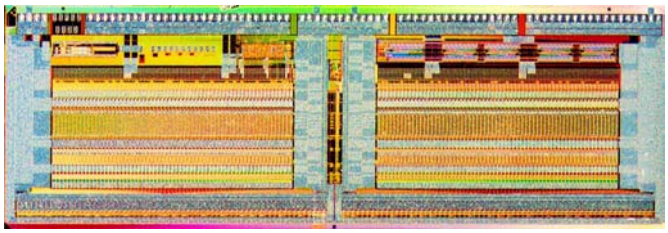

Figure 2: The HAL25 chip. Inputs from sensor are on top.

Since 2001, the MPW runs provide working chips but with a yield ranging between 98% and 8%. This issue has been fixed meanwhile, the engineering run providing about 3000 working chips (647 chips/wafer) with a yield ranging from 85 to 95%. Each module including 12 HAL25 chips, about 24 000 chips will be mounted inside ALICE, requiring an expected production of about 50 000 chips.

C. Chip cables

The HAL25 front-end chips are connected to the sensor on its input side by 128 input connections with a pitch of 80 µm, and to the hybrid on the opposite so-called output side by 78 output, power and control connections with a pitch of 125 µm. All these connections are provided by a single flexible chip-cable consisting of more that 200, 14 µm thick aluminium traces on top of a 10 µm thick polyimide foil. Minimum pitch is 80 µm. For easy TABing, fast testing, easy and safe handling and labelling, these chip-cables are fixed inside a plastic chip-frame or chip-carrier. Such a framed HAL25 chip as presented in figure 3, similar to a dia slide, plugs directly inside a dedicated test plug which connects onto the pad equipped extensions of the traces. The 128+78 connecting traces allow fast and safe test of the chip itself as well as of the TAB connections between the chip and the chip-cable. The pad equipped extensions are removed just before assembling the chips onto the hybrids [3], [7], [8], [9]. One should point out that this technology represents a technological break through in this range of pitches and in this application area.

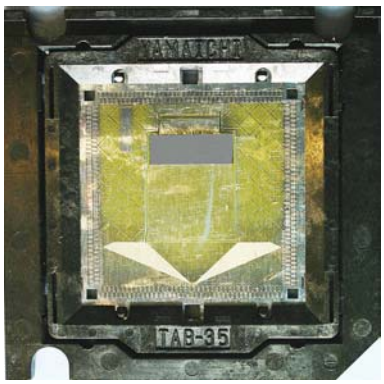

Figure 3: The framed HAL25 chip (grey rectangle) TABed on top of its chip-cable. Test pads appear along the outside of the chip-cable.

D. Hybrids

The hybrids are made of a two layer flex circuit, each layer having 30 µm thick aluminium traces on top.20 µm polyimide. Both layers are glued together and electrical connections are provided via TAB bondings between corresponding pads on the two conductive layers of the flex. A 5 layered carbon fibre-epoxy stiffener located underneath the HAL25 chips provides for mechanical stability and cooling distribution. The only passive CMS components provide signal lines adapting and power decoupling. This assembly provides optimal electrical, mechanical and thermal performances associated to a very low mass for good radiation transparency.

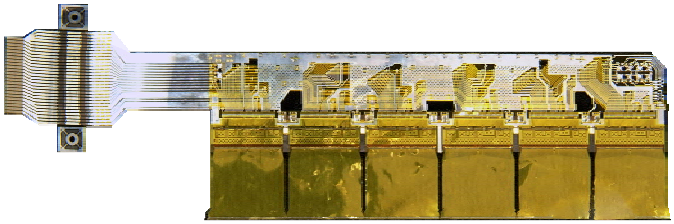

Figure 4: The hybrid supporting the FEE for 768 analogue channels.

Figure 4 shows a complete hybrid with the hidden HAL25 front-end chips and the stiffener underneath the main axis of the hybrid, the connecting circuits on the upper part with the connection to the outside by means of the connector top left

(removed after testing) and the input part on bottom connecting the 768 inputs of the HAL25 analogue channels to the corresponding strips of the sensor.

E. Assembling

The first assembling step is in fact TAB bonding of the HAL25 onto the chip-cables to provide finally tested chips on chip-frames.

The second step connects the so-called output side of these chips to the tested hybrid already equipped with CMS components. Once completed, this assembly is remotely tested by means of the connector.

The last steps connect one hybrid to the P side strips of the sensor and a second hybrid to the opposite N side strips.

Electrical testing of this assembled module provides data to be stored in the production database.

Micro-connections with a 80 µm pitch require sophisticated tools for accurate geometrical positioning and tuning of the components to be assembled. Semi-automatic bonding machine K&S was used for the early prototypes whereas Delvotech 6400 was used for the last module prototypes.

Even if made of preliminary passivated 350 µm thick chips and preproduction sensors, all five assembled modules are working.

Production of these nearly 2000 modules will be shared between two laboratories and industry.

IV. TESTS

After having been qualified for use by electrical testing, the detection characteristics of these modules have to be investigated. This means that one has to impact possibly calibrated radiation onto the sensor to investigate the corresponding output of the modules. We used sequentially Sr source input, laser light and two runs of beam tests. These latter provide obviously the most confident information. So we will focus on these last information available just a few days before this workshop.

The first run of beam tests in June 2003 was dedicated to single module investigation, the three available modules being used in sequence. The second run in September 2003 implemented a five-modules assembly allowing simultaneous read-out of four modules. This set-up was not only dedicated to single module investigation concerning gain, noise, dead channels a.s.o. but also to integration and spectrometer behaviour with geometric resolution and efficiency computation. Figure 5 shows this 5 modules assembly, each module being fixed in a so-called "flat" configuration inside a holding frame for test purpose. The whole assembly is then covered by a protective container shield against EMI and light.

F. Beam test readout

Operating such a module with the FEE being floating on different electrical potentials requires a sophisticated readout implementing floating transfer of all analogue and digital information in both directions. AC coupling operated by dedicated chips, ALCAPONE and ALABUF [10], developed in 0,25 µm technology is implemented in the readout assemblies.

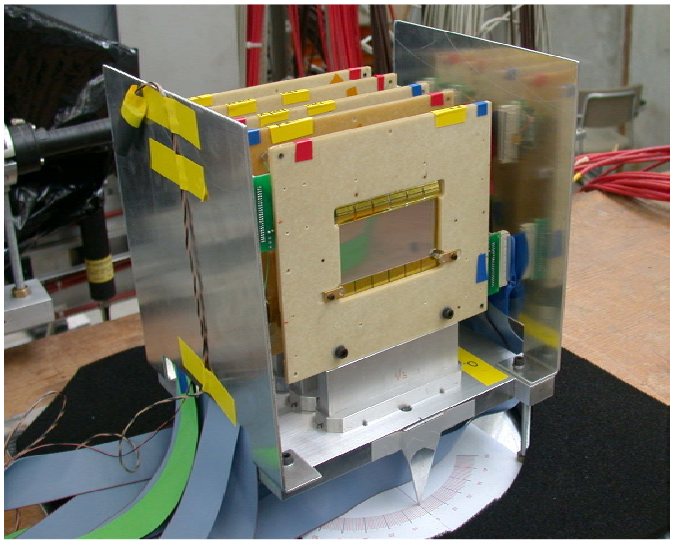

Figure 5: The five modules assembly for the beam test.

These readout assemblies used for the beam test are electrically similar to the final ones [11] which will have to be squeezed down in a very small space. Corresponding block diagram and main connections are presented in figure 6.

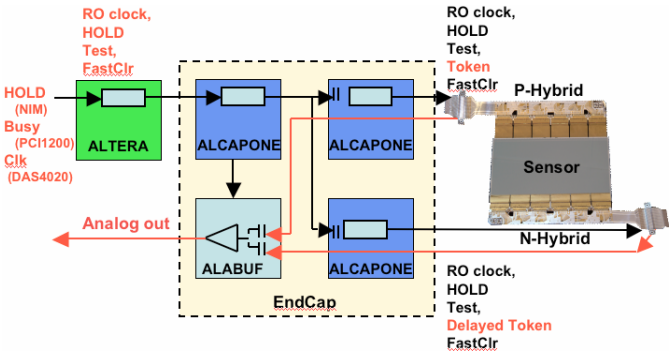

Figure 6: The module readout bloc diagram.

G. Beam test set-up

This multi-module set-up is intended to provide not only electrical performance evaluation but also geometric and efficiency information. To get multi-hit data, an iron target was placed in from of the set-up for some acquisitions. Finally, this run should allow comparison between different sensor providers and also comparison between modules assembled in different laboratories with different equipments.

Figure 7 shows the black container on the right, protecting the five assembled modules whereas the read-out boards are just laying left next to the detector modules. Trigger is located in the back whereas control and data acquisition, not presented here, are located in the control room.

Figure 7: The beam test setup, the modules are covered by black shielding, readout is on the left and trigger in the back.

The data taken during this one week run remain to be analysed in depth. Only very preliminary results could be produced up to now.

H. Results

Pedestal plots represent the output value for each strip averaged over several acquisitions as presented in figure 8. One can notice that the mean values of this pedestal are at mid-range of the 12 bit ADC in order to operate with positive as well as with negative signal outputs.

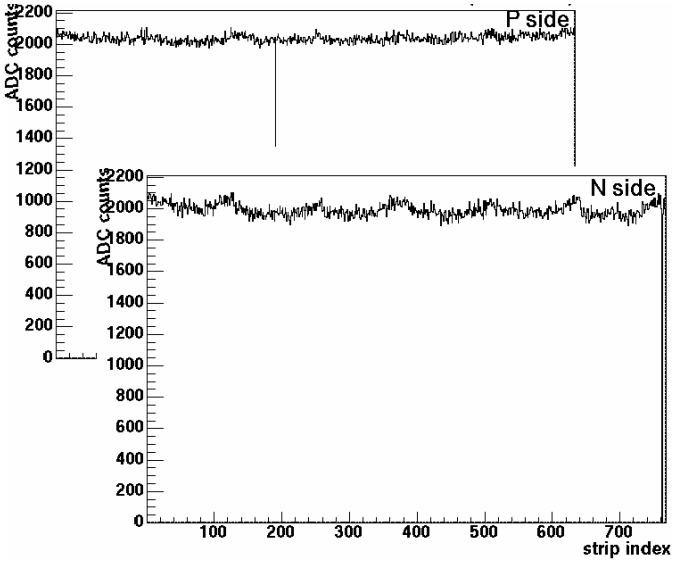

Figure 8: Pedestal of a typical module (SNC0003).

Noise represents the spread of these output values for each strip as presented in figure 9. One can notice that only a very few channels are very noisy. Nevertheless, noise baseline is significantly higher on the ohmic N-side than on the junction P-side. The lower noise performance on P-side is manufacturer dependant and should be improved. Moreover, common mode noise represents the most significant contribution to the noise. Both issues remain under investigation.

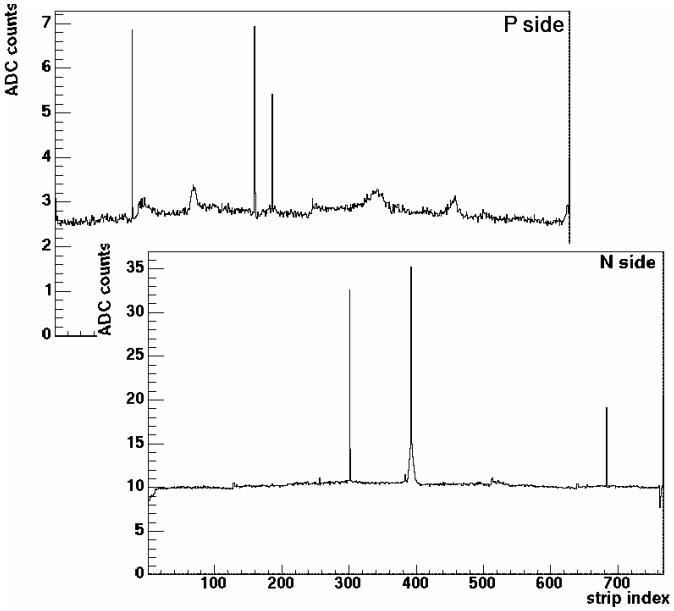

Figure 9: Noise of a typical module (SNC0003).

After having removed the common mode noise from the strip signal, the latter is processed with respect to the correlated noise in order to identify the clusters and to get the cluster charge. As presented in figure 10, the cluster charge distribution provides the typical Landau plot, peaking at 200 ADC units for MIP particles.

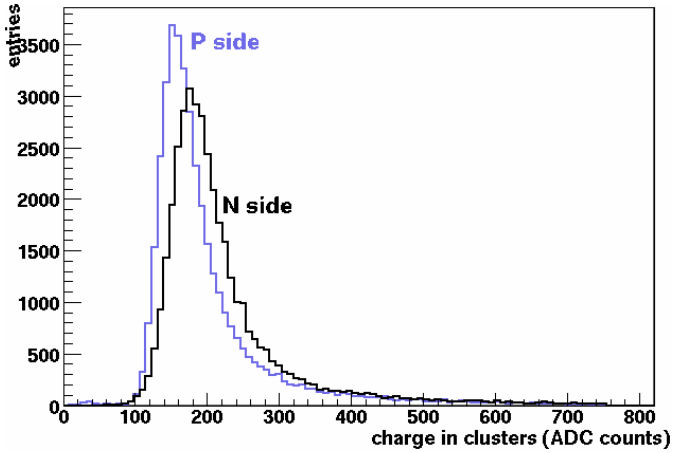

Figure 10: Cluster charge of a typical module (SNC0003).

Even with a symmetric charge collection on both sides as demonstrated on figure 10, the relative high noise level on the N-side of some modules, depending on the connected sensor, delivers a significantly lower signal over noise profile on N-side compared to P-side. The signal over noise ratio is presented in figure 11 for module SNC0003 and in figure 12 for module HNS0002 which is equipped with a different sensor and assembled in a different laboratory than SNC0003.

Charge matching performance is important to discriminate between real particle impacts and ghosts in high multiplicity interactions. Figure 13 plots the cluster charge collected on P-

side on the vertical axis whereas the cluster charge collected on P-side is plotted on the horizontal axis.

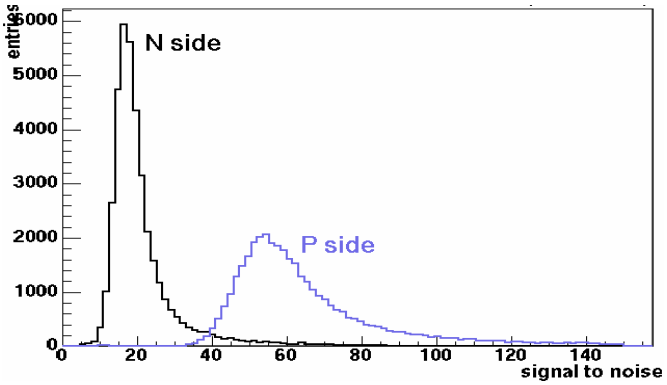

Figure 11: Signal over noise ratio of SNC0003.

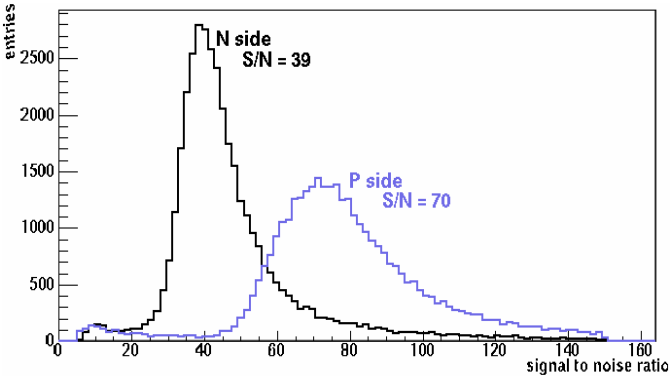

Figure 12: Signal over noise ratio of HNS0002.

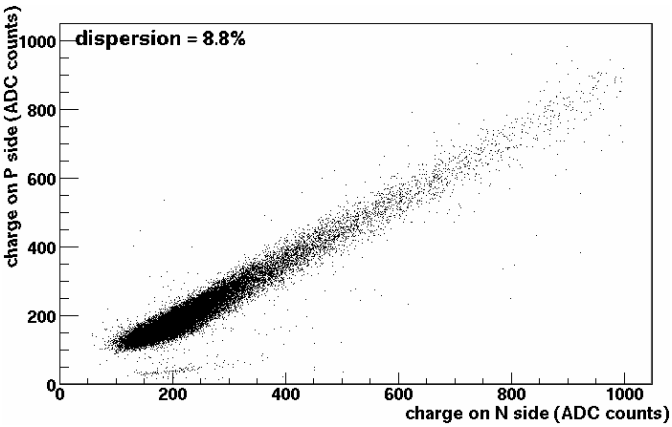

Figure 13: Charge matching of SNC0003.

Width of the dispersion, here 8.8%, is slightly lower on other modules, having a better signal over noise ratio.

V. Conclusions

This set of beam tests was intended to qualify the SSD modules for production. All the 5 available modules were working for the full one week test period in real operating conditions. No failure happened. System integration into real CERN background and multi-module operation registered no problem. Above the preliminary results presented here, analysis of the available data has to be obviously continued and correlation of the data taken simultaneously by the four modules should provide interesting complementary information on resolution and efficiency, even if similar information is already available from the past [1], [3].

Main specifications of the SSD front-end modules can be considered as achieved and production could start now. Second order issues like module noise on N-side, chip thinning, TABing automation, production rate, tests and diagnostics automation remain to be clarified before or during the ramping up of the module production. Delivery of sensors and front-end chips should no more be a bottleneck.

VI. References

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