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Structural defects caused by a rough substrate and their influence on the performance of hydrogenated nano-crystalline silicon n–i–p solar cells

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ABSTRACT

We present a cross-sectional transmission electron microscopy study of a set of hydrogenated nano-crystalline silicon n–i–p solar cells deposited by hot-wire chemical vapour deposition on Corning glass substrates coated with ZnO-covered Ag layers with various surface roughnesses. Strip-like structural defects (voids and low-density areas) are observed in the silicon layers originating from micro-valleys of Ag grains. A correlation between the opening angles of the textured surface and the appearance of these strips was found. We propose that in order to grow high-quality hydrogenated nano-crystalline silicon absorber layers for solar cell applications, the morphology of the Ag surface is a critical property, and the micro-valleys at the ZnO surface with an opening angle smaller than around 110° should be avoided.

1. Introduction

Hydrogenated nano-crystalline silicon (nc-Si:H) is a good absorber material for thin-film solar cells [1–3]. Controlling the quality of the material is of central importance in obtaining high solar cell performance. On the other hand, for such applications, silicon layers often have to be deposited on substrates with intentional roughness in order to achieve optical enhancement [4]. However, for nc-Si:H solar cells with the intrinsic absorber layers deposited with plasma-enhanced chemical vapour deposition (PECVD) techniques, it has been reported that substrate roughness may have an undesired effect on the quality of silicon layers, resulting in a detrimental effect on the output performance of solar cell devices.

Using techniques such as atomic force microscopy (AFM) a substrate surface profile can be obtained based on which one can deduce the root mean square (*rms*) value of the surface roughness. By comparing the *J–V* properties for nano-crystalline cells deposited on such substrates one observes a trend of decreasing V_{oc} with increasing *rms* roughness of the substrate surface. Such a trend has been reported previously on p–i–n cells with transparent substrates coated with rough ZnO by Nasuno et al. [5], and on n–i–p cells by the IMT group (Bailat et al. [6]), and a proposal of controlling the slope of the surface texture was given [5]. Such pioneering works raised questions fundamentally related to the physics of material growth and their influences on device performance, namely, why the variation of surface roughness influences solar cell properties such as V_{oc}, and how this is connected to the growth of nc-Si:H deposited on such substrates.

This question can be further broken down to four more detailed questions. Q1: is the substrate surface influence an interfacial effect or bulk effect? Q2: does the substrate roughness variation alter the properties of doped layers? Q3: do the voids often observed in the silicon layers deposited on such substrates also contribute to the decrease of V_{oc}, due to, for example, in-diffusion of impurities? And Q4: what are the criteria for a substrate to obtain maximum light-trapping ability avoiding any detrimental effect that could be brought about by suboptimal substrate surface morphology?

In this article we explore the possible answers for the above questions by investigating a dedicated series of samples. One unique characteristics of this set of samples is that the intrinsic layers were deposited with a plasma-free technique (hot-wire chemical vapour deposition—HWCVD), in which no energetic ions are involved. Using this deposition technique considerably simplifies the interpretation of the development of nc-Si:H on rough substrates, and therefore of the performance of devices developed on such substrates.

2. Experiment

The solar cells discussed in this contribution have the structure of Corning 1737 glass/rough Ag/ZnO/phosphorous-doped nc-Si:H n-layer/nc-Si:H i-layer/boron-doped nc-Si:H p-layer /ITO/Au grid. To study the influence of substrate surface morphology on the solar cell performance, nc-Si:H n–i–p solar cell samples were deposited under identical conditions on glass/Ag substrates with

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various roughnesses. Corning 1737 glass coated with texture-grown highly reflecting Ag or Ag:AlO_x layers was used as substrate. A single-target Ag or Ag:Al (1%) was used in an argon/oxygen ambient during sputtering. The surface roughness was varied by adjusting the substrate temperature. The thus-made substrates were kept in a dry N_2 cabinet at room temperature for about a day before being used for Si deposition. The silicon layers were deposited in a multi-chamber ultra-high vacuum system (PASTA). Doped Si layers were prepared using 13.56 MHz PECVD, whereas HWCVD was applied to fabricate intrinsic proto-Si:H and nc-Si:H. Two straight Ta filaments were used for the hot-wire deposition, through which a current of 10.5 A was passed, yielding a wire temperature of approximately 1850 °C in vacuum, as measured by a pyrometer. The ZnO and ITO layers were deposited by magnetron sputtering at room temperature, using ZnO:Al(1%) and In_2O_3/Sn_2O_3(10%) as the target material, respectively, and unless mentioned otherwise, with a typical thickness of ~100 nm for the ZnO:Al and ~80 nm for the ITO. The morphology of Ag surface was characterized by scanning electron microscopy (SEM) and atomic force microscopy. The structure of solar cells was studied with Raman scattering spectroscopy and cross-sectional transmission electron microscopy (XTEM). All the XTEM specimens were prepared in an identical process. Solar cell/glass sandwiches were made with silicon layers glued to face each other; they were first cut into thin slices in a direction perpendicular (90°) to the substrate surface; then polished to a slice of around 20 μm thickness, and then further thinned by an ion mill. A FEI Technai 20 electron microscope was used for the XTEM investigation. All the AM1.5 *J–V* data shown in this article were obtained with a WACOM dual beam solar simulator. An illumination mask was used to have a precise definition of the cell area. The same mask was also used for the deposition of the ITO top contact. Due to the finite thickness of the mask and the accompanying shadowing effect, the thus-measured J_{sc} values are slightly underestimated.

Ten pieces of Corning 1737 glass/Ag/ZnO substrates were prepared, with a different surface *rms* roughness varying from 13 to 135 nm. The samples were divided into five groups of two substrates that were loaded side by side in the same run. Table 1 lists the surface parameters of these substrates, as well as the data for an Ag (200 nm)/ZnO (100 nm)-coated Asahi U-type glass as a reference. The AFM images of four of these substrates are shown in Fig. 1.

Table 1
Substrate parameters derived from 10 μm × 10 μm AFM images.

Group	Sample name	Substrate	*rms* (nm)
A	A_1	S_A_1	73
A	A_2	S_A_2	133
B	B_1	S_B_1	13.4
B	B_2	S_B_2	88.2
C	C_1	S_C_1	61
C	C_2	S_C_2	111
D	D_1	S_D_1	67
D	D_2	S_D_2	135
E	E_1	S_E_1	83
E	E_2	S_E_2	92
R	R	Asahi_U	32

3. Experimental results

3.1. Electrical properties: substrate surface rms roughness dependence of open-circuit voltage (V_{oc}), diode quality factor (*n*) and dark reverse saturation current density (J_0)

Fig. 2a shows the dependence of AM1.5 open-circuit voltage (V_{oc}) on substrate *rms* roughness. For samples made under

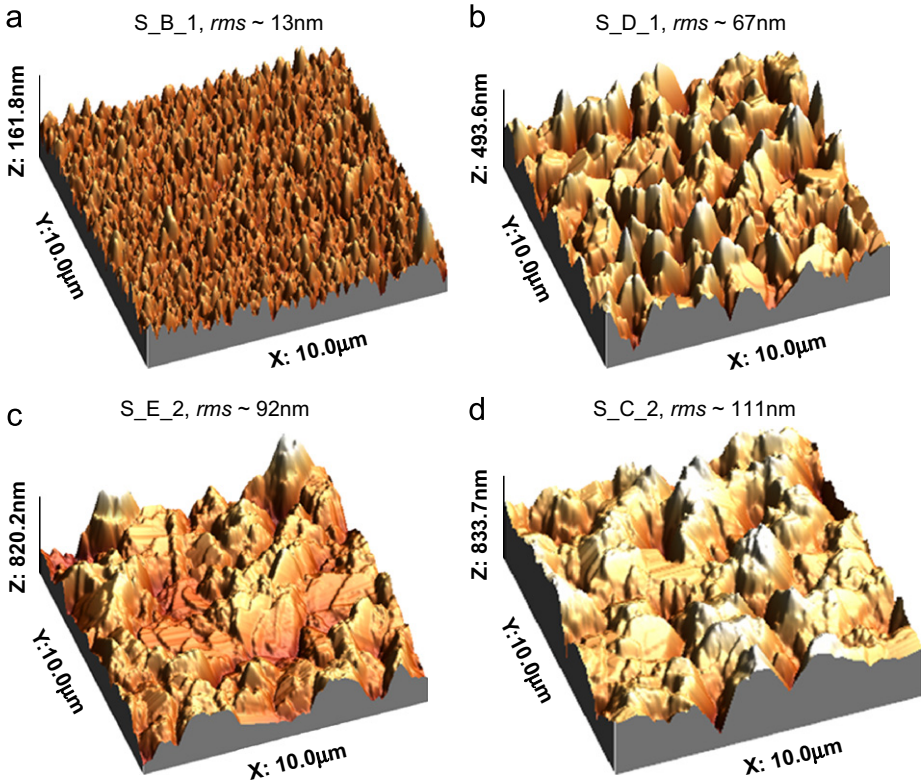

Fig. 1. AFM pictures of glass/Ag/ZnO substrate with different surface roughnesses.

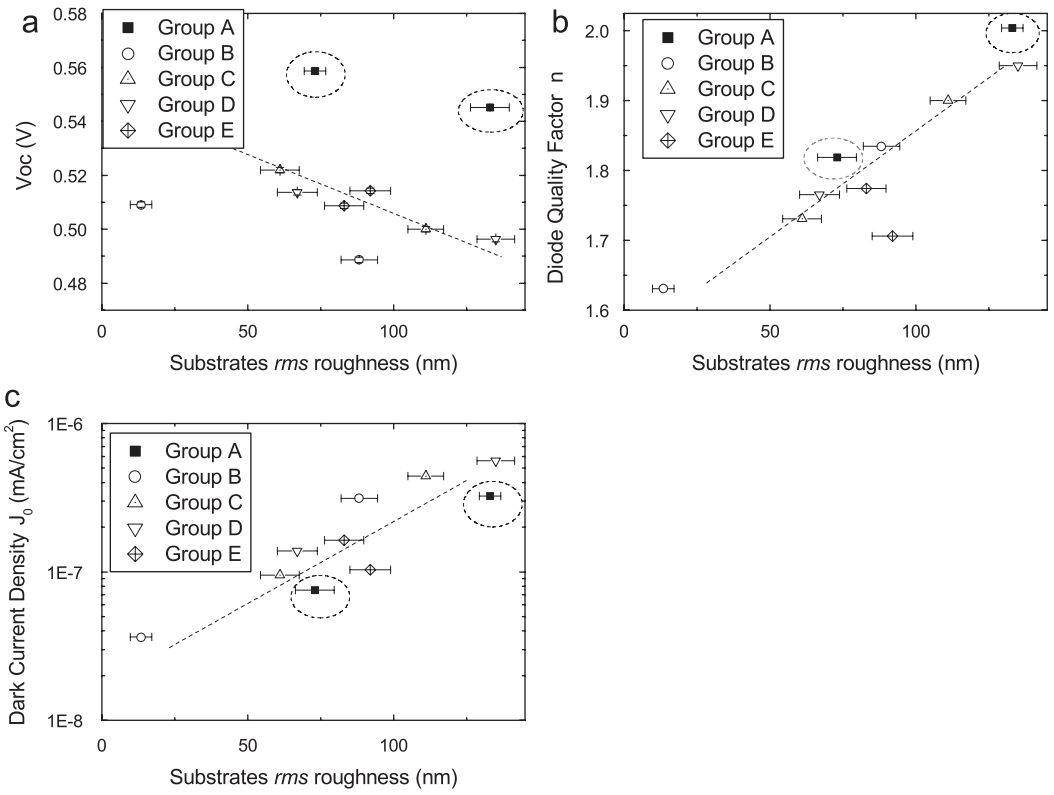

Fig. 2. Correlations of V_{oc}, J_0 and n of working cells with substrate surface roughness *rms* value. Points in the dashed circles are cells made with a double n-layer. Lines are guides to the eyes.

identical conditions, a clear trend of decreasing V_{oc} with increasing *rms* roughness exists. The samples with their data points surrounded by a circle (group A) were made with a profiled n-layer (a "double n-layer") using a two-step deposition: the first step was done at standard n-type a-Si:H deposition conditions to a thickness of around 5 nm, and the second step was done at conditions for n-type nc-Si:H, to a thickness of around 27 nm. The conditions for the second step were identical to those used for the deposition of the n-layers of the samples in the other groups. From Fig. 2a it is clear that this group of samples shows higher V_{oc}. Figs. 2b and c give the values of the reverse saturation current density J_0 and the diode quality factor n deduced from the dark J–V curves (Table 2). For all the 10 samples studied, the trends of the observed increase in both parameters as a function of the *rms* roughness are clearly visible, although the samples in group A show somewhat lower J_0 and higher n values than the other samples with a similar substrate *rms* roughness.

To study this remarkably clear correlation between Ag/ZnO substrate surface roughness and the solar cell J–V characteristics, especially the J_0 and n values, the samples are compared within each group. In this way, we can minimize the possible influence from any run-to-run variation of the deposition parameters.

3.2. Structural properties

3.2.1. Structure properties of Ag/ZnO substrate

For the Ag layer used for these experiments, a strongly ⟨111⟩-preferred crystalline orientation are found for all the samples by XRD measurements (not shown). With an increase of substrate temperature during sputtering, the ⟨111⟩ preference enhances as well. This correlates with an increased surface *rms* roughness of the Ag layer. Since all the ZnO layers were deposited in the same condition and their thicknesses were kept the same for each group of samples, their influence on our discussion is limited.

Table 2
Fitted n and J_0 values for the diode J–V curve subtracted from the dark J–V curves of two solar cell samples in each group listed in Table 3.

Group	*a*	*b*	*c*	*d*	*e*
rms (nm)	133	88.2	111	135	92
n	2.09	1.77	2.08	2.10	1.78
J_0 (A/cm^2)	1.69×10^{-7}	2.22×10^{-7}	4.39×10^{-7}	5.10×10^{-7}	2.49×10^{-8}

3.2.2. TEM examination: strip-like area in the nc-Si:H i-layer

Figs. 3a–c show the bright-field TEM images of the two samples in group A. The substrate *rms* roughness for these two samples are 73 (a) and 133 nm (b and c). In the images of the sample made on the rougher substrate, one can clearly see low-density lines appearing in the silicon layers. Those lines, or the strip-like areas, are the places where very few or no atoms are present in the atomic network during the Si growth. Some of these strips have a width of nearly 100 nm (as that shown in Fig. 3c), which is wide enough to form a micro-shunting path between the front contact (or p-layer) and the Ag/ZnO back contact. As a reference, Fig. 3d shows the structure of a sample deposited under the identical condition but on a substrate with a nearly flat Ag/ZnO substrate (*rms*∼4 nm). Clearly, no strips can be observed in this sample.

Strip-like areas with various sizes are observed in the TEM images of many of the examined samples in this series, and they can be classified into two categories: (1) those that start in the ZnO and Ag layers like those shown in Figs. 3b and c and (2) those

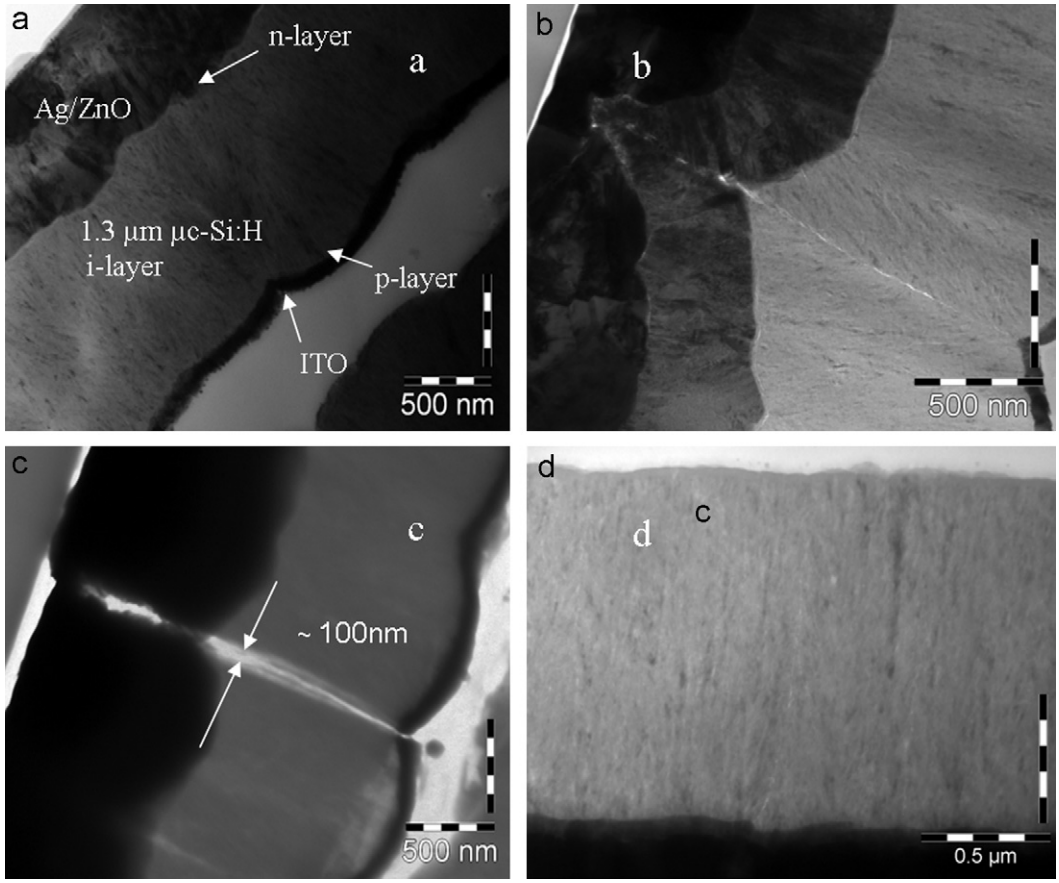

Fig. 3. Cross-sectional TEM images of nc-Si:H n–i–p cells made on Ag/ZnO-coated Corning 1737 glass. (a) Sample S_A_1, (b) sample S_A_2, (c) another picture of sample S_A_2 for cracks study and (d) a nc-Si:H n–i–p sample made on a nearly flat Ag/ZnO substrate with a substrate surface *rms* roughness of ~4 nm. The total thickness of the silicon layers in all the samples are around 1.5 μm.

that start only in the silicon layers, a image of this type of strips is shown in Fig. 4. For the strips that already appear inside the ZnO and Ag layer, it is often observed that the strips become a hollow area in the silicon layers; whereas for those that start in the silicon layers, it is often hard to distinguish whether they are hollow or are filled with silicon with low atom density, since the width of these strips is often smaller than those in category 1.

One common feature of these two types of strips in this series of samples is that once formed they develop along the Si growth direction toward the top surface of the n–i–p structure, with a tendency to decrease in width, as seen from the TEM picture. Some of the strips with a small width show closure near the top surface, although the collision of the individual silicon columns can still be clearly seen.

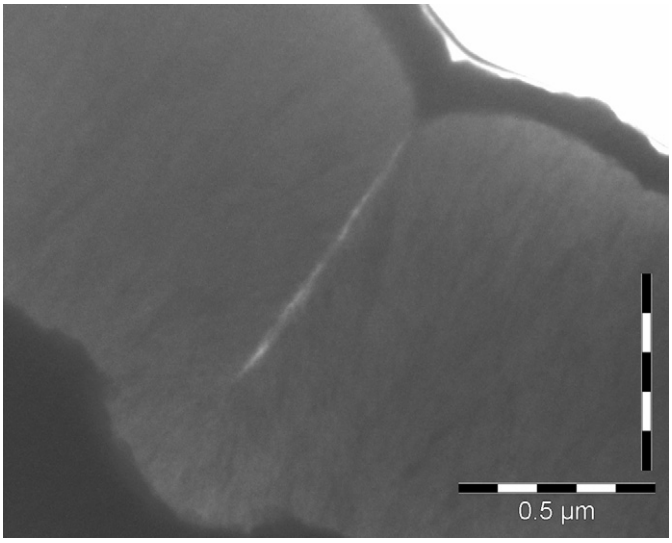

Fig. 4. A cross-sectional TEM image of a nc-Si:H n–i–p cell showing strip-like structural defect formed in the silicon absorber layer.

3.2.3. *Raman spectroscopy examinations*

A common explanation for the V_{oc} difference of nc-Si:H cells is the difference in the i-layer crystallinity. The most straightforward way to check the i-layer crystallinity is by means of Raman scattering spectroscopy at the outer surface of the sample. Due to the limited penetration depth of the excitation light, this, however, gives structural information only in the uppermost part of the layer stack. Fig. 5a shows the normalized Raman scattering spectra for samples in groups B–E, where the substrate *rms* roughness varies from 13.4 to 135 nm. The spectra were taken employing a 514.5 nm wavelength argon laser beam incident from the p-side of the sample, on the area without the ITO coating. The penetration depth for light with this wavelength is around 200 nm for nc-Si:H material; therefore the Raman spectra give structural information on the whole p-layer (~20 nm thick) and a considerable part at the top of the i-layer. Except for a small shift in the

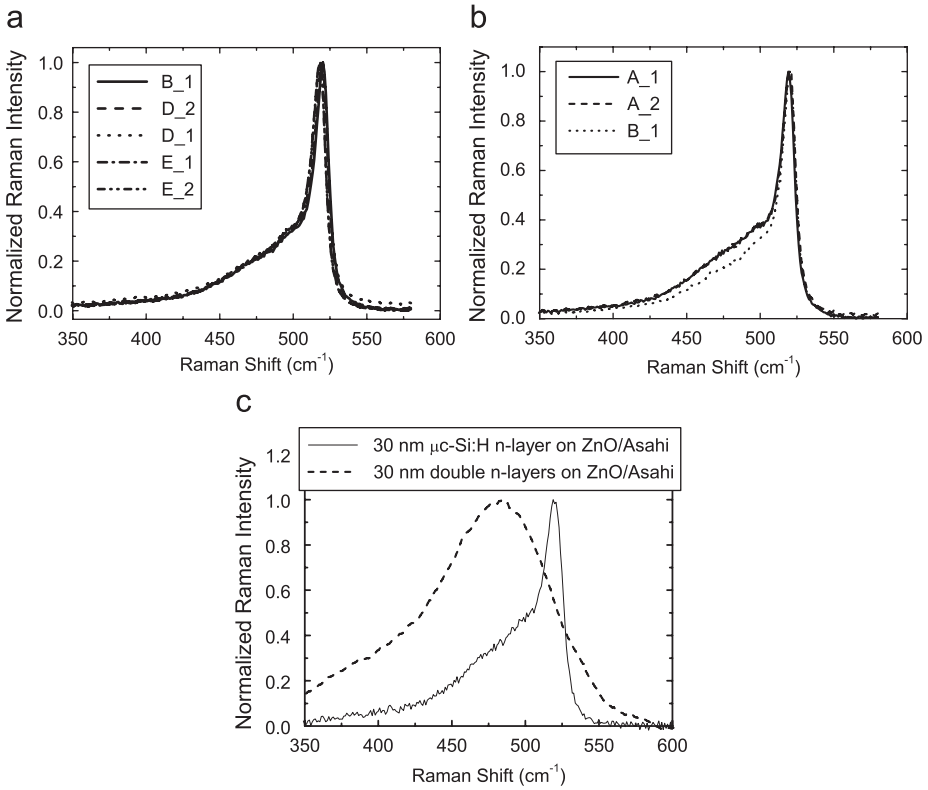

Fig. 5. Raman scattering spectra on the p-side of (a) the samples with a single n-layer, (b) the samples with a profiled n-layer, (c) Raman spectra of a ~30 nm thick double n-layers (light grey line) and of a ~30 nm thick single n-layer (black line). Both are deposited on ZnO-coated Asahi-U TCO glass substrates; the substrate signal has been subtracted.

peak values, due to the different calibrations between measurements, the normalized intensities for all the samples exactly overlap. For the two samples made with a "double n-layer" (group A, shown in Fig. 5b), the Raman spectra show clearly higher intensity in the spectral range 400–510 cm^{-1} than the other samples (represented by sample B_1), which indicates a higher amorphous content for this group of samples. Again, no difference can be observed between the two samples in that group. Therefore, it is justified to assume that the observed differences in V_{oc} for different surface morphologies are not likely to be due to differences in crystallinity of the i-layers.

4. Discussion I: possible reasons for the V_{oc} deterioration for solar cells developed on rough Ag/ZnO substrates

4.1. Connection between J_0, n and V_{oc}

The V_{oc} of a thin-film silicon p–i–n (including n–i–p) diode has a fundamental connection with the diode quality factor n and the dark saturation reverse current density J_0, namely

$$V_{oc} = \frac{nkT}{q} \ln\left(\frac{J_{sc}}{J_0} + 1\right) \quad (1)$$

If there is no carrier transport barrier between the doped silicon layers and the contacts, such as the barrier found at the interface between ITO and the p-type nc-Si:H layer [9], the J_0 and n values deduced from the dark J–V characteristics give information on the quality of the silicon layers and their interfaces. In the case for drift-current-dominated carrier transport, an increased diode quality factor indicates an increased carrier recombination in the bulk of the i-layer, if the Fermi level and the electronic band gap in the i-layer remain unchanged.

4.2. Issues related to the influence of short-circuiting paths on the value of V_{oc}

The high density of large voids observed in the TEM images of the samples made on rough substrates contributes to the low yield of working cells, as we have shown in our previous publications [11]. But is it also responsible for the lower V_{oc} of these samples? To answer this question, quantification of the density of these short-circuiting paths (SCPs) is necessary. It is known that the current that flows through those paths has a linear correlation with the bias voltage, and it contributes to a large extent to the differential resistance deduced from the J–V characteristics of solar cells at zero bias voltage (R_{sc}). This suggests us to use R_{scD} (R_{sc} deduced from the dark J–V measurement) to represent the density of the SCPs. But, since the transport losses such as the recombination of thermally generated carriers in the intrinsic layer also contribute to the value of R_{scD}, we shall clarify to what extent this will influence the R_{scD} values. To verify the validity of this representation, an R_{scD} versus *rms* roughness curve is shown in Fig. 6. Clearly, R_{scD} decreases with an increase of *rms* roughness. To estimate the influence from the i-layer recombination, $R_{scdiode}$, which is deduced from the fitted diode current density−voltage (J_{diode}–V) curve in the voltage range $V > 0.2$ V, is also shown. The n and J_0 of the J_{diode}–V curves are taken from the values shown in Figs. 2b and c. One can see, in the entire range of *rms* values, that R_{scD} is more than 10 times smaller than $R_{scdiode}$, which confirms that carrier recombination in the i-layer has a negligible influence on R_{scD} of this set of samples.

Using this concept, namely that R_{scD} is correlated with the areal density of SCPs in a cell, we study the R_{scD} dependence of V_{oc} for the two samples in group A (Fig. 7). It can be seen that for cells with R_{scD} below around 100 Ω cm^2, V_{oc} decreases linearly with

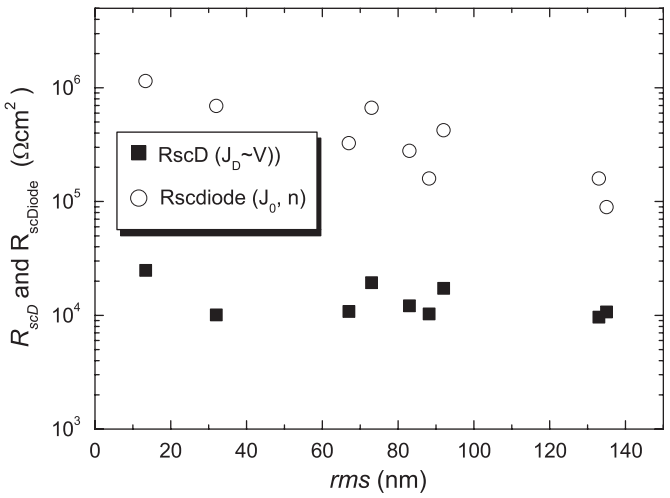

Fig. 6. R_{sc} versus *rms* dependence for the best cell of the samples listed in Table 1.

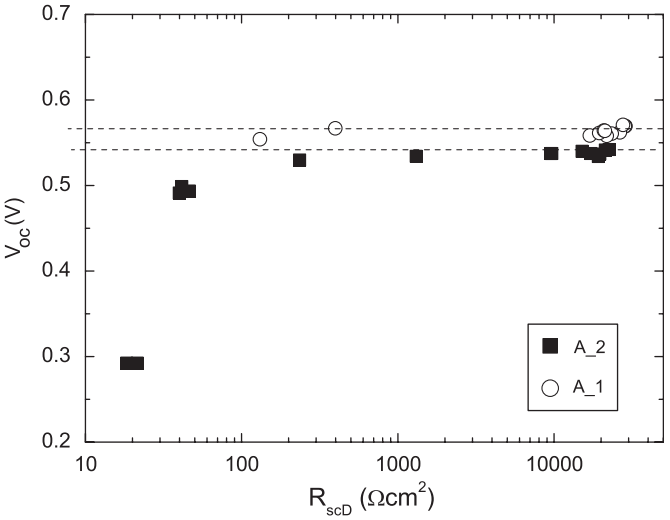

Fig. 7. V_{oc} and R_{scD} correlation of the two cells in group A.

decreasing R_{scD}, which indicates the dominance of SCPs (with shunting resistance of R_{sh}) for those cells. For cells with R_{scD} higher than around 100 $\Omega\,cm^2$, V_{oc} becomes saturated even though R_{scD} increases by more than two orders of magnitudes, i.e. from around 100 to $2\times10^4\,\Omega\,cm^2$. The nearly 30 mV difference between the two saturated V_{oc} values, 0.54 and 0.57 V for the higher and lower *rms* sample, respectively, indicates that R_{scD} is irrelevant to the V_{oc} difference between these two samples. That is to say, the difference in V_{oc} between these two samples is not due to the shunting resistance introduced by the different areal densities of the observed SCPs [11].

4.3. Possible substrate rms roughness dependence of effective areas for J_0 calculation

The dark saturation current density J_0 was calculated by fitting the linear part of $\log(J_{dark})\sim V$ curves, assuming that the effective area through which the electric current is flowing is the same for different substrate surface roughnesses. However, the interface area through which carriers inject into the silicon layers in cells deposited on a smoother substrate is probably different from that in cells deposited on a rougher substrate. It is therefore possible that the relatively higher effective area of the cells on a rougher substrate increases the dark saturation current, which in turn results in a lower V_{oc} than on a less-rough substrate. Since we have measured the substrate surface 3D profile by AFM, we can estimate the surface area of each substrate, and therefore, calculate to what extent this area enhancement influences the cell V_{oc}.

Fig. 8 shows again the *rms* roughness dependence of J_0 (squares), but with additional data points where the J_0 was recalculated with the effective area integrated from the AFM picture for each substrate (triangles). Also shown in this figure is the J_0 obtained with a simulated area based on a pyramid assumption (illustrated in the inset of Fig. 8) with the substrate lateral feature sizes and the *rms* heights as input parameters (circles). Although the enhancements of the substrate effective area by a rough surface indeed result in a small increase in the J_0, ~5% on average, it can be seen that the trend of increase in J_0 with substrate *rms* roughness is not at all influenced. Further more, the fact that the diode quality factor *n* shows a similar trend with the substrate *rms* roughness (Fig. 2c) confirms that the decrease in V_{oc} is not due to the substrate effective area variation; otherwise the *n* values would be more or less constant for this set of samples.

4.4. Issues related to the possible differences in the crystallinity of the intrinsic nc-Si:H layers

The difference in crystallinity between samples in group A (with double n-layer) and the samples in the other groups (B–E, with a single nc-Si:H n-layer) can be well explained by the influence of the doped layer (n-layer) on the growth of the nc-Si:H i-layer. This is supported by studying the Raman scattering spectra (shown in Fig. 5c) of n-type nc-Si:H layers used for this set of samples. Both samples shown in this figure were deposited on ZnO-coated Asahi-U TCO substrate. One can see that the ~32 nm thick double n-layers (used for samples in group A) together form essentially an amorphous layer, whereas the ~27 nm thick single nc-Si:H n-layer (used for samples in groups B–E) has high crystallinity. Due to the lower crystallinity of this "double" n-layer of the samples in group A, the intrinsic nc-Si:H that grow on top of it are less crystalline, as shown in Fig. 5b,

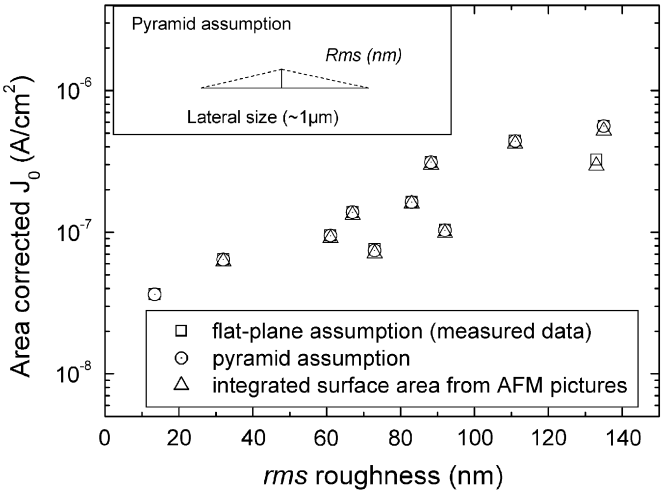

Fig. 8. Substrate *rms* roughness dependence of the current density J_0, with the effective area estimated from flat-plane assumption (open squares, measured data), pyramid assumption (open circles) and the integrated surface area from the AFM pictures of Corning/Ag/ZnO substrate (open triangles).

resulting in a considerable higher V_{oc} for these samples than for those in the other groups. This again indicates that control of the structure of the doped nc-Si:H is an important factor in the optimization of nc-Si:H solar cells.

As shown in Section 3.2 the Raman scattering spectra did not show difference between samples in all the groups with substrate *rms* roughness (*rms*) variations in a wide range. This means that the observed correlation between V_{oc} and *rms* is not caused by the silicon crystallinity variations near the p/i-region, including that of the p-layer and the top ~150 nm i-layer. To distinguish the difference in the crystallinity in the bulk of i-layers is, however, not possible at this stage. Therefore we compared the cross-sectional XTEM images of the samples made on different substrates. Based on the pictures that we have obtained, we did not find any difference in crystallinity among samples in the groups B–E, and between samples within group A.

4.5. Possible influence from the p-type nc-Si:H layers

It can happen that the p-layers that are intended to be nc-Si:H turn out to be amorphous in structure. This is due to the sensitivity of boron-doped nc-Si:H to small variations in the deposition parameters and substrate conditions [9]. Since the p-layer deposition conditions for this set of samples are the result of a thorough optimization, and all the samples had a post-annealing treatment in a N_2 atmosphere to improve the p/ITO/Ag top contact, the influence from this aspect is not considered to be an issue. Besides, the fact that Raman spectra obtained on samples in each group completely overlap also rules out a possible crystallinity difference in the structure of p-layer and p/i-interfaces.

It is, however, possible that impurities, such as moisture, oxygen, or metal elements, diffuse through the pinholes, such as those shown in the XTEM images (Fig. 3b), and cause changes in the electrical properties of the p/i-interfaces. However, this is considered not to originate from the p-layer itself.

4.6. Possible influence due to nonlinear J–V contribution of the microvoids

Although microvoids filled with conductive material are not the cause for the difference in V_{oc} of the cells, as we have shown in Section 4.2, unintentional doping caused by impurities such as moisture and oxygen accumulated or diffused into these voids may very well influence the transport properties of the intrinsic nc-Si:H layer. Besides, structural defects near the boundaries of silicon columns are likely to contribute to a higher electronic defect density than the dense parts of the i-layer and this, as a consequence, can enhance carrier recombination. Such influence may not immediately short circuit the cell, but contributes to the deterioration of p–i–n diode, namely the diode quality factor n and the dark reverse current density J_0. While writing this paper, the IMT group just reported a study on the *J–V* contribution of the cracks (similar to the term voids we used in this article) by assuming an extra diode in the equivalent circuit of the solar cell, namely a "bad diode" with a diode quality factor fixed as 2 (denoted as n_2), and dark reverse current density m^*J_{crack} (denoted as J_{02}) where m represents the density of cracks per unit area (cm^2). With this assumption, they obtained a good fit to the experimental AM1.5 and dark *J–V* curves [12]. For our sample series, we can test whether this "bad-diode" assumption also hold for our HWCVD samples. Since for each group of samples the properties of silicon layers are identical (good diode) and the only difference between them is the amount of structural defects (voids or cracks, or fissures) caused by different degrees of substrate roughness, we can simply subtract the *J–V* curve of the two samples and obtain the information for n_{diff} and $J_{0,diff}$ purely contributed from the structural defects (assumed to be the "bad diodes"). Fig. 9 shows the result of such analysis. One can see that indeed for the two cells in group A, the "bad diode" seems to have an n value of around 2, indicative of a recombination-dominated diode behaviour. Applying this method to samples in all the five groups of this series, we obtain a table where n_{diff} and $J_{0,diff}$ change with substrate surface *rms* roughness (taken as the larger values in each group). We see that for samples made on rougher substrates ($rms > \sim 110$ nm), the diode quality factor n_{diff} is just around 2, while for samples made on smoother substrates ($rms \leqslant \sim 90$ nm) n_{diff} is somewhat lower (~1.8). This result shows the validity of the "bad-diode" assumption for the contribution of voids or low-density strips in n–i–p cells.

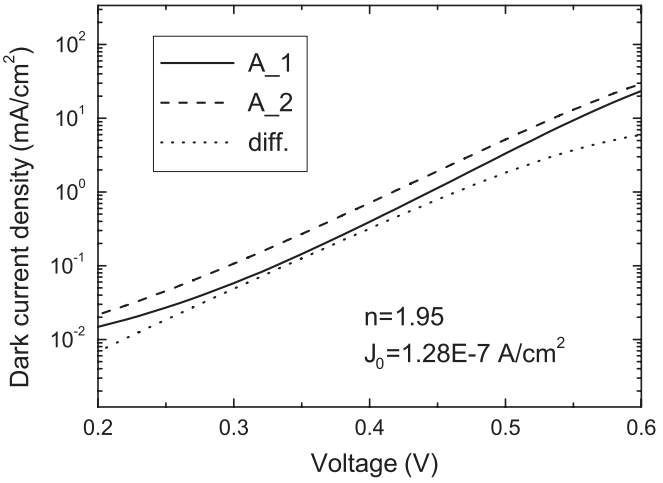

Fig. 9. *J–V* of cell A_1 (solid line) and cell A_2 (dashed line) in group A and the difference between them (dotted line). Diode quality factor n and dark reverse current density obtained for the dashed line are given in the graph.

Table 3
Summary of the factors influencing the V_{oc} of a nc-Si:H n-i-p solar cell.

Possibilities	Influences on V_{oc}
Short-circuiting paths that are observed in the XTEM images of cells deposited on a rough Ag/ZnO substrate	Not for cells with $R_{scD} > \sim 100\,\Omega\,cm^2$
Influence of the differences in effective areas on the dark saturation current density	No
Difference in the structure of p-type nc-Si:H and the p/i interface layers	No
Difference in the electronic properties of the p-type nc-Si:H layer and the p/i interfaces	Not likely. The p-layer was optimized and their structure is independent of substrate roughness
Difference in amorphous volume fraction in the i-layer	Possible, but not due to the p-side of the i-layers
Difference in the electronic properties of the n-type nc-Si:H layer	Possible, n-layer may have different structures due to its possible discontinuity on a rough substrate
In-diffused impurities, especially through the pinholes formed in the cells deposited on a rough substrate	Yes
Difference in the electronic defect density of nc-Si:H i-layer	Yes

4.7. Summary of the factors influencing cell V_{oc}

Before going to the next section, we summarize our discussion on the possibilities that can influence the V_{oc} of the cells in this *rms* series in Table 3.

To answer the questions raised in the introduction part, we summarize our discussion as follows. Whether the substrate surface influence on V_{oc} is an interfacial effect or bulk effect?—the substrate surface morphology influence on V_{oc} can be both bulk and interface effect, but in the case of forming fissures in the i-layer, the bulk effect likely dominates. Whether the voids often observed in the silicon layers deposited on such substrates also contribute to the decrease of V_{oc}, due to, for example, an in-diffusion of impurities?—Yes. Both the in-diffusion path and highly defective region may be located near the voids and low-density areas of the intrinsic layer. They can increase the density of electronic defects and trapping centers, therefore resulting in increased carrier recombination in the i-layer. The experimental results obtained on our samples support the "bad-diode" model proposed by the IMT group [12]. Namely, the electrical influence of such strip-like structural defects on the solar cell *J–V* characteristics may be simulated by a residual diode with a diode factor of around 2.

The crucial question is what are the criteria to obtain a substrate with the maximum light-trapping ability without the possible detrimental effect brought about by improper substrate surface morphology? We will try to discuss this issue in the next section.

5. Discussion 2: nano-crystalline silicon growth on a Ag/ZnO-coated substrate

From the XTEM images shown in Fig. 3 and the pictures published by other groups (for instance by Meier et al. [13] and Nasuno et al. [5]), it is clear that under optimized deposition conditions for nc-Si:H growth (~250 °C substrate temperature), in the first stage of deposition that the silicon crystallites tend to grow almost perpendicular to the local surfaces of the substrate. The continuous increase in film thickness is accomplished by the formation of crystallites elongated in the same direction as those that already exist within the film. As a result of this epitaxial-like film growth ("nano-epitaxy"), columns are formed with their *z*-axis roughly perpendicular to the original local surface of the substrate.

5.1. Silicon growth on a flat surface

If the substrate surface is perfectly flat, the columns will continue developing in their original direction, with a tendency to increase in diameter as long as the micro-environment around the film growing front allows for that. At least two factors will limit the expansion of the silicon crystal columns in the lateral direction. Firstly, the silicon-containing precursors, mostly believed to be SiH_3, must have enough mobility on the growing surface in order to find a suitable place to be connected to the silicon lattice. This is a general requirement for the formation of silicon crystallites in the growth of silicon thin films. Secondly, there must be enough space for the widening of these columns, i.e., the density of the columns must not be too high. Based on our study on nc-Si:H deposited by hot-wire CVD on a flat substrate (Corning 1737 glass) with R_H~0.95 and at a substrate temperature around 250 °C, if the deposition parameters are held constant, this second factor is almost solely determined by the density of nucleation sites formed already in the initial stage of film growth.

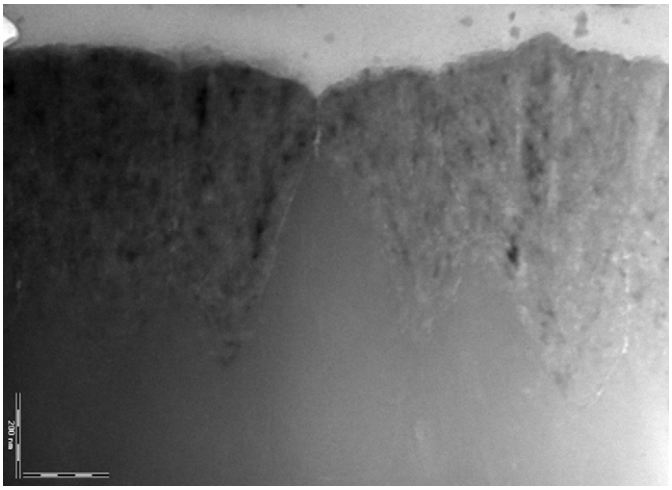

Fig. 10. TEM image of a nc-Si:H material sample deposited on top of amorphous a-Si:H layer on Corning 1737 glass. The scale bar shown in the picture is 200 nm.

For example, in most nc-Si:H materials deposited on an a-Si:H surface, large cones are formed near the substrate. This is due to the low nucleation density formed on (or in) the a-Si:H under those deposition conditions. With an increase of layer thickness, these silicon cones develop along the layer growth direction and can finally become columns by colliding with each other at a distance far from the substrate (~0.5 μm or more), as is shown in Fig. 10. The films containing both columns and cones are figuratively named as having a "pencil-box" structure [14].

Using a highly crystalline thin nc-Si:H layer, or a "seed layer", normally deposited with a high hydrogen dilution ratio [15], the density of nucleation sites can be greatly enhanced, and therefore the diameter of the silicon columns (the "pencils") can be significantly decreased. Based on this understanding, Bailat et al. [14] proposed a nuclei density model to generally describe the R_H [defined as $H_2/(H_2+SiH_4)$ gas flow ratio] dependence of cell V_{oc}, in which the importance of the changes in the average amorphous volume fraction in this heterophase region (where the cones appear) is stressed. We comment here, however, that this nuclei density model is not sufficient to describe the general dependence of V_{oc} of nc-Si:H cells on R_H, since in their model the crystallinity difference in the bulk of the i-layer was not taken into account, as Bailat et al. themselves mention in their publication. One can easily see that this is indeed the case in the *rms* roughness series presented here. The two samples in group A have a higher amorphous volume fraction in the n-layer than the samples in the other groups (groups B–E), which will likely result in some elongation of the incubation phase (the heterophase) of the intrinsic nc-Si:H layer near the n/i-interface. According to the nuclei density model, this would be the reason for the higher V_{oc} observed on these two samples. However, we also observe a lower Raman crystallinity (*Xc*) of these two samples (Figs. 5a and b), which is similar to that of the i-layers deposited with a lower R_H ratio. Since the excitation laser impinges from the p-side of the n–i–p stacks and the laser light cannot penetrate even half of the i-layer thickness, contributions from the material in and near the n-layers cannot contribute to the Raman spectra. The higher V_{oc} of these two samples can thus be better explained by the higher amorphous volume fraction in their i-layers.

5.2. Silicon growth on a rough surface

For nc-Si:H layers developing on top of a rough Ag/ZnO substrate, some additional factors are involved. Firstly, the

properties of the substrate material, such as the chemical reactivity and lattice structure, will influence the initial growth of silicon. Since we are discussing Ag/ZnO substrates with all the ZnO layers grown under identical conditions, influences from variation in substrate material will be limited. But we have to keep in mind that during the growth of a silicon film by PECVD, due to the conductive nature of this type of substrate, there will be differences in the local electromagnetic (EM) field near the substrate surface compared to the situation of a flat and insulating glass substrate. This influence from the substrate may play a role during deposition of the n- and p-type nc-Si:H layers that are plasma deposited before and after the nc-Si:H i-layer. For the HWCVD-deposited i-layer, the influence of the EM properties of the substrate is negligible.

Since, as we have shown previously, the n-layer acts as a seed layer for the growth of nc-Si:H i-layer in the n–i–p stack, the possibility of a variation of the n-layer structure brought about by the roughness of the substrate surface has to be considered. In a high-frequency (RF or VHF) plasma environment, a stronger EM field is present at the higher points (the tips) than at other places on the substrate surface. The likely result of this is a different chance of forming silicon nucleation sites on a tip than in a valley of the substrate surface. Within the resolution limit of the TEM pictures for this set of samples, we cannot clearly find differences in the density of small crystallites in the very thin n-layers. However, since the influence of this possible structural inhomogeneity of the n-layer on the growth of intrinsic nc-Si:H is our major concern, it is equally of interest to study the density of nucleation sites inside the i-layer, where the silicon crystal columns start to develop (where the tips of the "pencils" are located). TEM pictures containing both rough and flat regions were studied for this purpose. One of the pictures is shown in Fig. 11, from which one can indeed see that there are fewer crystallites above the flat region at the substrate/silicon interface (dashed white arrow) than above a rougher region (solid white arrows). The nc-Si:H crystalline columns that develop on the flatter surface further show a larger width than those developing on top of the rougher regions. It seems that there is a trend that silicon cones are more densely distributed near the high point of the substrate. This observation indicates that at least under these deposition conditions, the structural inhomogeneity of the PECVD-deposited n-layer can have an influence on the development of the nc-Si:H i-layer, even though there is no strong EM field at all during the growth of a hot-wire-deposited i-layer.

5.3. Formation of voids

For Ag layers sputtered at a very high substrate temperature, Ag (poly-) crystals with acute angles formed between the local crystal surfaces and the substrate plane are often observed in the TEM pictures. When two or more such Ag crystals are adjacent to each other, sharp valleys are formed between them, accompanied with very small opening angles [10]. Silicon grown in these valleys is typically accompanied with large voids located in the middle of the valleys, in which no silicon atoms exist. A picture showing this phenomenon is given in Fig. 12, where the width of the void is estimated to be around 120 nm. (Note that for the sample examined in this picture, no ZnO layer is used.) Voids of this size may be large enough to short circuit the complete device, if they extend through the entire i-layer [11].

One of the possible reasons for the formation of such voids is the limited trench coverage ability of silicon growth, which is mainly due to a higher growth rate near the upper surface of the valley than on the inner walls. As illustrated in Fig. 13, during Si deposition the thickening films developing around the upper surface of the valley meet each other before the valley is filled, leaving a large void in the middle of the valley. A similar explanation was used by Sakai et al. [7] for the voids observed in a-Si:H layers. We add here that the strong influence of nucleation sites on the growth of nc-Si:H and the possible inhomogeneity of nuclei density of the thin n-layer (deposited by PECVD) for this set of samples may magnify the chances of forming voids. Fig. 14 gives a schematic explanation for this situation (as a typical example, the substrate is drawn with a V-shape opening). In the lowest part of the valley, where Si nuclei density appears to be lower (due to a combination of the limited surface diffusion coefficient of adatoms and a possible influence of EM field on the local density of layer growth precursors), there is a high chance that layer growth will not start immediately; instead, nc-Si preferably grows on the side walls, where a higher density of nuclei is present, and easily closes the entrance to the trench before filling it completely. As a result, a void is formed below the point where the silicon growth fronts meet.

Fig. 11. XTEM picture of a nc-Si:H sample. Arrows and "*T*" letters indicate the origin and the width of columnar silicon, respectively. The dashed arrow indicates the place where silicon grows with a lower nucleation density.

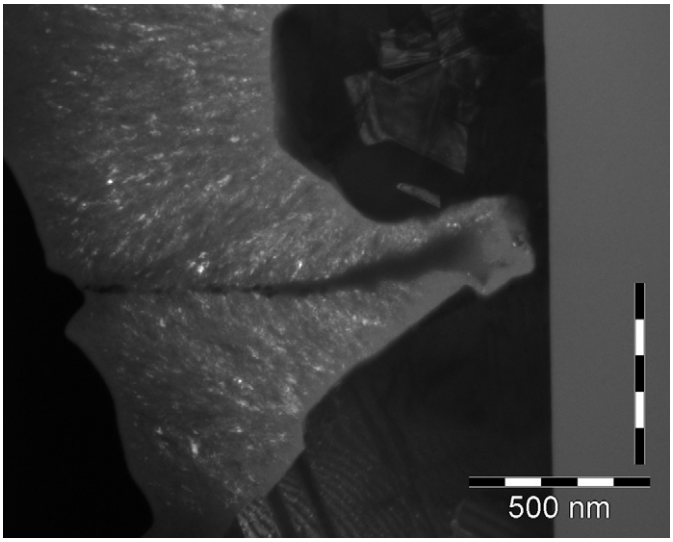

Fig. 12. nc-Si:H i-layer grown on top of a ~30 nm nc-Si:H n-layer-covered Ag substrate. No ZnO layer was used for this sample between the Ag and the n-layer.

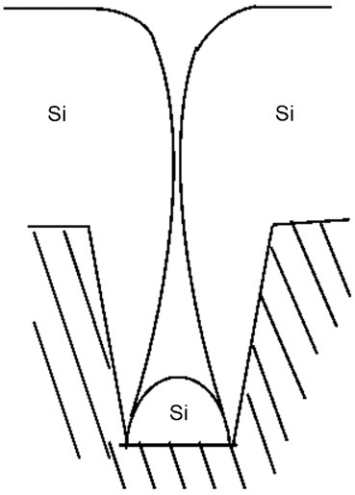

Fig. 13. Schematic cross-section of silicon growth in a trench with high aspect ratio.

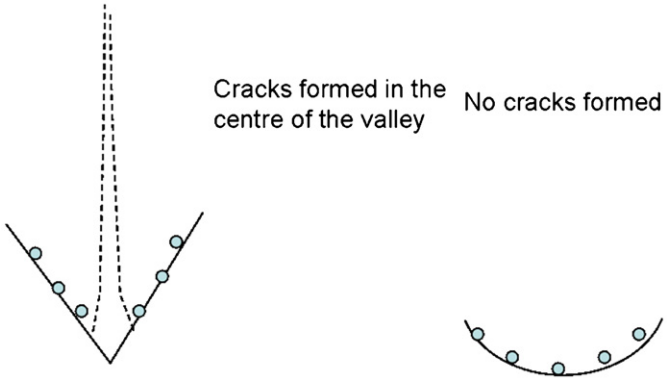

Fig. 14. Cracks may form due to the inhomogeneous distribution of silicon nuclei in the initial stage of silicon growth, or due to the structure of the seed layer, in this case of a PECVD-deposited nc-Si:H n-layer.

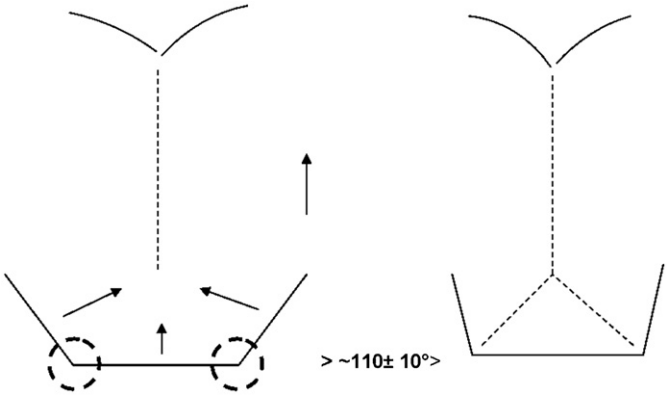

Fig. 15. Voids appear at the corners with unfavourable opening angles.

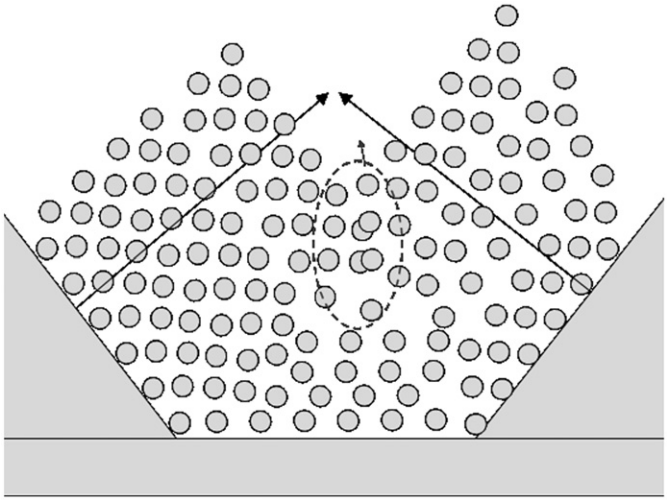

Fig. 16. A proposed model based on stress-forming silicon growth fronts and H etching during deposition.

Obviously, the substrate morphology dependence of the Si structure is determined by the geometry of the substrate local surface. It has been reported that nc-Si:H solar cells deposited on dry etched (by plasma) [16] or wet etched (by a HCl solution) ZnO [17] containing U-shaped craters on the ZnO surface show better performance than those made on as-deposited ZnO, typically containing V-shaped valleys. This can be explained by Fig. 14 as well: due to the change of substrate surface morphology, silicon nucleation near the bottom of U-shape valleys becomes easier, resulting in an increased density of Si nuclei on the bottom of the valley, which in turn suppresses the formation of voids.

One important feature of the voids observed in this set of samples is that once they are formed, they tend to develop along the growth direction and extend further into the bulk of the i-layer, with a trend of decreasing in width, as measured from the TEM images. Most voids are found to continuously develop up to the top surface of the p-layer. Based on the analysis given in the previous section, it is obvious that this type of voids should particularly be avoided in a solar cell device.

Besides the reasons shown above, there might be another explanation for the formation of such voids. This is based on the diagrams shown in Fig. 15. There seems to be a correlation between the appearance of the voids and the angles that form between Ag polycrystals. In valleys with an opening angle larger than a certain value, no voids are formed. This angular threshold has been found to be around 110°.

In Fig. 16 we show a possible explanation for the formation of such voids. Assuming that silicon develops layer by layer on top of the surface of the valley, the local films will grow freely until the growth fronts from different plates meet. As soon as they meet, there will be stress created in the silicon network. Due to the high density of atomic hydrogen present during the CVD process, the strained Si–Si bonds can be etched away, resulting in regions with a low density of silicon atoms—a void is therefore formed in that region (the black arrows in Fig. 16: layer growth direction; the area encircled with a dashed line: atoms that are easily etched away by H). As long as the layer continues growing in the same direction, stresses are constantly formed near the corner of the layer growth fronts; therefore the voids will continue to develop along the layer growth direction.

By controlling Ag deposition conditions, a surface containing microwells or valleys with low aspect ratio and wide opening angles is obtained. It is observed in TEM pictures of silicon films on these surfaces that the presence of voids is reduced or completely eliminated (Fig. 3a).

As a summary, Fig. 17 gives the observed angular dependence of the width of voids estimated from the TEM pictures. We note that the angular threshold (110°) as marked in the

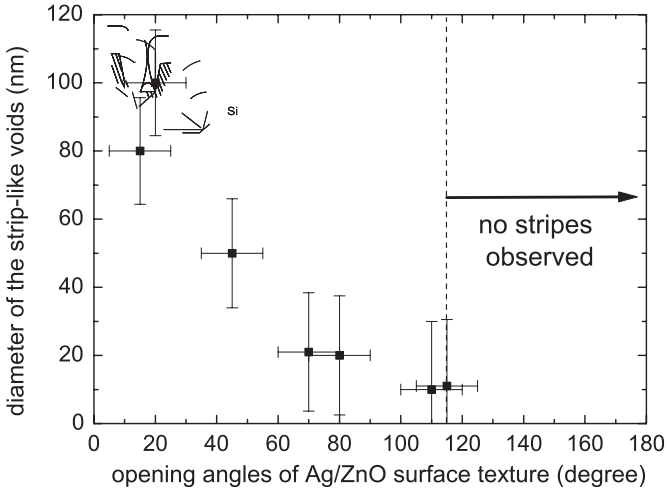

Fig. 17. Correlation between the opening angle of the Ag/ZnO surface texture and the width of the microvoids (white strips) determined from the TEM images of the sample series listed in Table 1.

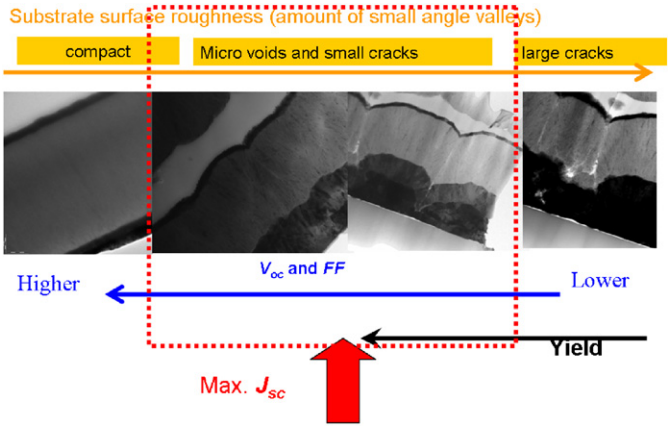

Fig. 18. TEM images of nc-Si:H n–i–p solar cells deposited on (from left to right) flat, medium rough and very rough glass/Ag/ZnO substrate. The total thickness of the silicon layers for all the samples shown in this picture is around 1.5 μm.

figure might also be related to the material growth technique and conditions.

6. More general discussion: a complete diagram for nc-Si:H n–i–p cell developed on rough Ag/ZnO substrate

Based on the discussion in Ref. [11] and Sections 4 and 5, a diagram of a set of TEM images of nc-Si:H n–i–p solar cells deposited on (from left to right) flat, medium rough and very rough glass/Ag/ZnO substrates is shown in Fig. 18. The total thickness for the silicon layers for all the samples shown in this picture is around 1.5 μm. Since the highest AM1.5 current density is obtained on cells made on a medium rough substrate [8], the best single junction nc-Si:H solar cell efficiency made in house is also obtained in that region (8.6% without encapsulation, a cell with a reverse hydrogen profiling [18]). Further improvement in cell efficiency would not only require an enhancement of the optical trapping, but also a modification of the substrate surface morphology, in order to suppress the detrimental effect of rough substrate surface on the quality of silicon layers.

As a guide for the substrate development, we suggest that the local surface of the substrate should have an opening angle larger than a certain threshold or the distances between the adjacent micro-cliffs are wide enough so that the collision plane of the tilted silicon columns is far from interfaces or even beyond the thickness of i-layer. Meeting these criteria while maintaining the maximum light-scattering ability, an "ideal" substrate for thin-film nc-Si:H solar cells can be found. We note that the value of this angular threshold may depend on the techniques and conditions for silicon deposition. For nc-Si:H layers deposited with hot-wire CVD using hydrogen-diluted SiH_4 at a substrate temperature of around 250 °C, this angle is found to be around 110°.

7. Conclusions

By studying the nc-Si:H n–i–p solar cell samples made on Ag/ZnO substrates with different *rms* roughnesses, we have gained the following knowledge.

The substrate roughness has a large influence on the structure of nc-Si:H. In the case of very rough Ag substrates (obtained by sputtering Ag layers at a high substrate temperature, >350 °C in our experiments, with *rms* roughness value larger than around 130 nm) the subsequent deposition of ZnO and Si layers fails to conformally fill the submicron cavities formed by the large Ag crystal grains. As a result, pinholes with diameters larger than ~100 nm appear in the silicon layers, which are responsible for the low yield of solar cells deposited on this type of substrate [11].

For nc-Si:H cells developed on a Ag/ZnO substrate with a medium rough Ag layer (with *rms* value around 30 to around 130 nm), the yield of working cells is high, but the obtained V_{oc} is lower than that of cells grown on smoother substrates. The two most probable reasons are: (i) microvoids formed in the silicon layers near the Si/ZnO interface propagate into the Si i-layer, due to which impurities such as moisture or oxygen may accumulate, changing the Si electrical properties near that area and (ii) a higher electronic defect density is caused by the higher grain boundary density in the nc-Si:H layers when grown on a rough substrate due to the collision of silicon columns. In both cases the morphology of the substrate surface plays an important role, and it is therefore essential to control it in order to further improve the efficiency of nano-crystalline silicon thin-film solar cells.

Strip-like structural defects (voids) with widths of about a few to a hundred nm have been identified in silicon layers, and in ZnO or Ag layers. The strips generally develop along the deposition direction and extend into the bulk of the Si intrinsic layer or through the silicon layers up to the top surface of the n–i–p structure, with a trend to decrease in width. The widths of the strips are found to be dependent on the local opening angle of the Ag substrate surface. For the strips starting in the silicon layer, the highest opening angle of the local ZnO surface for the formation of these strips is found to be approximately 110°.

Complicated substrate surface profiles and limited trench coverage ability by CVD are considered to be responsible for the formation of the structural defects observed in the silicon layers. Further, the lack of silicon nuclei near the bottom of the valleys may increase the chance of formation of such voids. Applying a substrate surface modification process, such as chemical etching, as in the case of using ZnO substrate [16,17], or by adjusting the Ag deposition temperature, as in our case, the density of such voids can be minimized, and the solar cell performance can be improved [18].

As a guide for further development, a complete diagram for the structure of nc-Si:H n–i–p cell developed on rough Ag/ZnO substrate with different roughnesses has been composed.

Suggestions for further optimization of the substrate surface morphology are given.

We note that although our study has shown a strong influence of voids and defective areas between silicon columns on nc-Si:H solar cell performance, the solar cell V_{oc} is not merely determined by the density of such areas. Also the crystalline volume fraction of the silicon columns and the use of special interfacial layers influence to a large extent the solar cell performance, especially V_{oc}, as shown by our data.

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[10] It is also possible that such narrow valleys in the Ag layers are cracks formed after Ag sputtering, especially for those deposited at high temperatures due to the high strain formed in such layers. Since the Ag/ZnO substrates had been kept at room temperature for around a day and were heated again before being used for solar cell fabrication, if there are cracks formed in the Ag layer due to high strain, most possibly they have been formed before the Si deposition, so that our explanations and the proposed model are not influenced. Besides, we have also seen (as shown in Fig. 4) that there are voids/cracks formed inside the silicon layers, which should not be correlated to the Ag expansion.

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