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A FAST LINEAR GATE CIRCUIT

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An electronic gate circuit is described, which is linear for pulses up to 10 V over an impedance of 200 Ω. The gate-pulse width is determined by an external clipping cable and can be varied from 500 ns down to 40 ns. The input can be of either polarity. The gate incorporates a fixed, well defined dead-time of about 50 μs, which assures stable operation also at high counting rates.

1. Introduction

A gate circuit transmits an input pulse, when a trigger pulse is also applied to the circuit. A linear gate should not modify the pulse-height spectrum of the input pulses. Both the transient of the trigger pulse when no input pulse is applied (pedestal), and the feed-through of the input pulses when the gate is closed, should be sufficiently small.

Within our knowledge all gates in the nanosecond region, thus far published, are basically pure crystal diode gates. Generally these are non linear for smaller pulses and also a pedestal cannot be avoided in most cases[1,2]).

For fast gates a major difficulty arises at high counting rates by the time jitter between the pulse which keeps the gate open (gate pulse) and the signal pulse. This jitter can introduce an important variation in output pulse height. Part of this jitter can be introduced by the circuitry preceding the gate, but also the gate-pulse generator can give a considerable contribution.

The present circuit is of a symmetrically balanced type, which is capable of giving a zero pedestal. It is linear over its whole region of operation, down to zero pulse height. The variation in output pulse height, caused by the jitter from the gate-pulse generator is suppressed by setting an upper limit to the counting rate the gate can feed through. For that purpose a fixed dead time is introduced in the circuit. When the output spectrum is recorded with a multichannel kicksorter, which has normally a rather long dead time, the overall counting rate is hardly decreased by the dead time in the gate circuit.

2. The Circuit

The basic element of the gate circuit consists of two 1 : 1 pulse transformers in series, separated by two fast crystal diodes††† (fig. 1). When the gate is not triggered the diodes are biased off by a positive voltage. A suitable negative gate

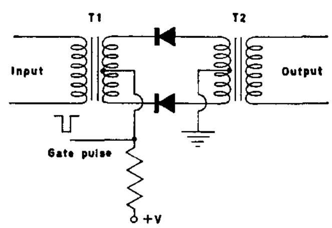

Fig. 1. Basic diagram.

pulse applied at the centre tap of the secondary windings of T1 drives both diodes into a highly conducting state, so opening the gate. When the circuit is well balanced, the pedestal arising from the gate pulse will be negligible, as the

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††† The idea of this transformer gate is originally from L. J. de Vries, I.K.O., Amsterdam.

1) A. V. Tollestrup and J. B. Lindsay, CERN Report 58-20 (1958).

2) E. L. Garwin, Rev. Sci. Instr. 30 (1959) 373.

currents in the loops give fluxes in T2 which are equal and of opposite sign. If the point of operation of the diodes in the conducting state is chosen well (with the right gate pulse height) then the variations in impedance of the two diodes can be made about equal and, of course, they are of opposite sign. So the total impedance of the intermediate loop is practically constant for not too high pulses. Also it is not too serious when the compensation is not complete, as the diode resistance is only a fraction of the impedance of the windings. Therefore the gate can be linear over a wide range of input pulse heights.

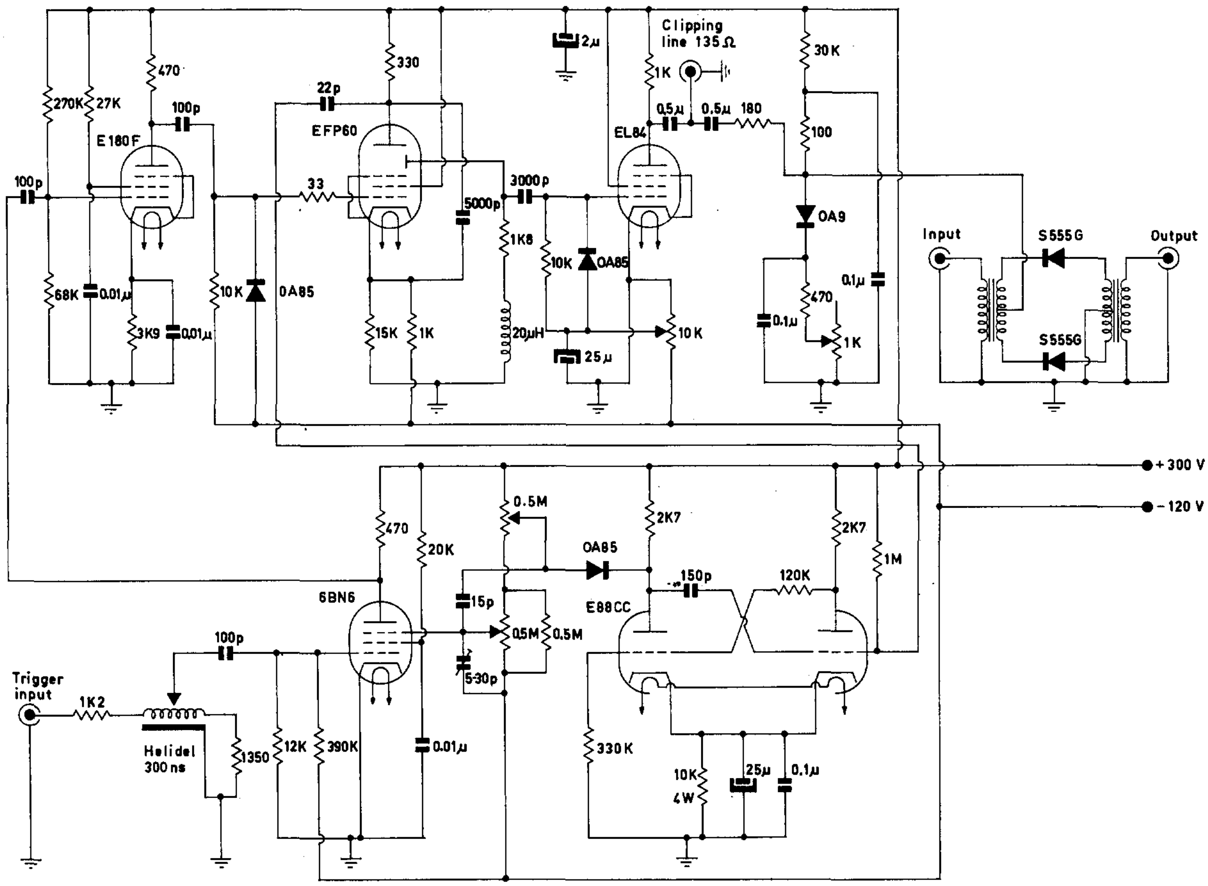

Fig. 2

The complete diagram is shown in fig. 2. The trigger pulse must be positive and at least 5 V high and of 60 ns half width. With the variable delay line the difference in time between the trigger pulse and the signal pulse can be adjusted. If necessary, the signal pulses can be given a constant delay with a suitable length of cable. The trigger pulse is applied to the first control grid of the 6BN6. In the quiescent state the tube is biased off by this grid. When the univibrator (E88CC) is not running, the trigger pulse is given through to and amplified in the E 180F, which in the quiescent state draws a current of 15 mA. The rise time of the pulse is also improved.

The gate-pulse generator consists of a EFP60 pulse generator, followed by a pulse shaper (EL84). The dynode pulse of the EFP60 (with the coupling to the EL84 removed) is about 500 ns long, 120 V high and has a rise time of 20 ns. This pulse drives the EL84, which is normally biased off, into a highly conducting

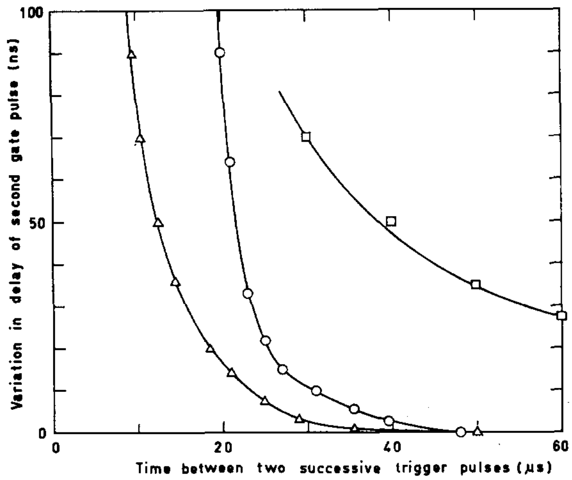

Fig. 3. Influence of counting rate on the jitter. The circles represent the circuit in normal operation, the triangles with the EFP60 triggered with a 13 V pulse and the squares are measured with the resistances in the cathode of the EFP60 increased by a factor 10.

state. The resulting anode pulse is flat topped and has a rise time of 8 ns. With a clipping cable the gate pulse can be given the desired length. With a resistor network the clipping cable is matched and the height of the pulse at the anode of the 0A9 diode, with the gate disconnected, is reduced to 30 V. The diode removes almost entirely the positive part of the clipped pulse.

For higher counting rates the time distance between the trigger pulse and the gate pulse is no more constant, but increases with increasing counting rate. This effect is shown in fig. 3 for two successive trigger pulses, as a function of the distance between these pulses. The repetition frequency of the double pulse generator was 500 Hz. The effect can be diminished by increasing the trigger-pulse height on the EFP60. The origin of this variation is the bias shift of the EFP60 cathode, as is shown by reducing the current through the cathode voltage divider down to 0.8 mA.

To overcome this difficulty the dead time is introduced in the circuit. With the differentiated anode pulse of the EFP60 a univibrator (E88CC) is triggered. The negative univibrator pulse of 50 μsec duration is d-c coupled to the second control grid of the 6BN6, which is then cut off completely, so no main trigger pulse can be given through. During the time the univibrator is flipping back the 6BN6 is in an intermediate position. To keep this time as short as possible, the coupling capacity in the univibrator is made small and the anode current is high (20 mA). Also, by the biased crystal diode only the lowest 10 V of the anode pulse is given through to the 6BN6. So the resulting rise time of the back edge of the pulse applied to the 6BN6 is reduced to 0.2 μsec.

The pulse transformers in the gating element are made with ferrite potcores (Philips Ferroxcube 3B). Each coil consists of 6 windings of H.F. Litze wire (12 $\times$ 0.08 mm). Between the coils a static shield is placed, to reduce capacitive feed-through. The transformers must be wound with great care in order to achieve the highest possible symmetry. As a slight assymetry is almost unavoidable, the remaining small pedestal can be removed by placing a small inductance in series with one of the two diodes.

A number of different types of diodes has been tested for the gating element. The best results gave the diodes Philips 0A9 and Transitron S555G.

One is free to select the impedance of the in- and output cables. In our experiment the signal pulses are first amplified with a Hewlett Packard distributed amplifier, so an impedance of 200 Ω has been chosen. The cables have to be matched properly at their far ends, as the gating element represents no constant impedance.

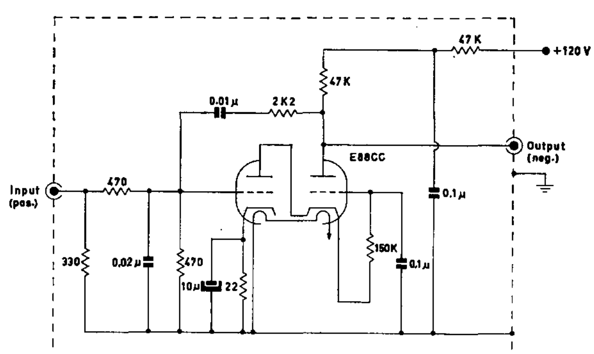

Fig. 4. Pulse lengthener and low noise preamplifier.

To be able to select the output pulses with a multichannel kicksorter, the pulses have to be stretched to about 2 μs. A crystal diode pulse lengthener is non linear for small pulses, therefore a passive R-C-stretcher is preferred, even with the inevitable loss of pulse height, (fig. 4). The pulses are then amplified with a low noise cascode preamplifier with a gain of 12 and an equivalent noise resistance of 250 Ω. After amplification with a standard 0.5 μs pulse amplifier the pulses can be recorded with the kicksorter.

3. Performance of the Circuit

The linearity of the gate has been tested with a mercury-switch pulse generator (fig. 5). The signal-pulse length was 12 ns, and the gate-pulse length 40 ns. The gate is linear up to 11 V input pulses. This is also about the bias voltage of the diodes. For pulses up to 11 V the feed-through of the signal pulse when the gate is not triggered is 0.3%. For higher pulses the feed-through increased rapidly. The remaining pedestal has the appearance of the strongly differentiated gate pulse and is 70 mV high.

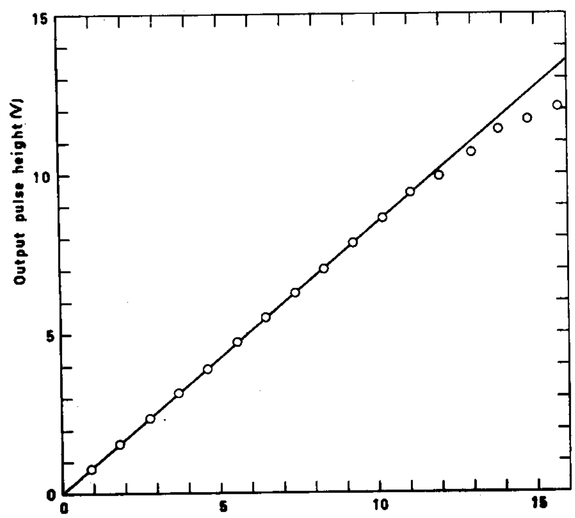

Fig. 5. Linearity of the gate.

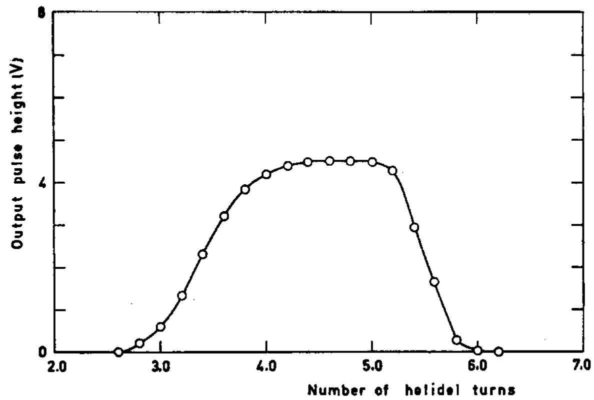

Fig. 6. Output pulse height versus helidel setting. One turn represents 20 ns.

In fig. 6 is shown the output pulse height as a function of the time delay between the trigger pulse and the signal pulse, for a gate-pulse width of 40 ns. The plateau of the curve is 15 ns, so a considerable jitter from the preceeding circuitry can still be tolerated.

It is evident that the polarity of the input and/or output pulses can easily be changed.

The circuit has been used quite satisfactorily in different experiments, performed with the Synchro Cyclotron of the CERN.

For some applications it can be useful to note that this gate can also be used in a reversed way. By inverting the polarity of the diodes and by driving a constant current through the diodes the gate is always open, except when the gate is triggered and the diodes are biased off by the gate pulse.

Acknowledgements

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