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A novel structured plastic substrate for light confinement in thin film silicon solar cells by a geometric optical effect

M.M. de Jong^a, J.K. Rath^{a,*}, R.E.I. Schropp^a, P.J. Sonneveld^b, G.L.A.M. Swinkels^b, H.J. Holterman^b, J. Baggerman^c, C.J.M. van Rijn^c, E.A.G. Hamers^d

^a University Utrecht, Debye Institute for Nanomaterials Science, Nanophotonics-Physics of Devices, P.O. Box 80.000, 3508 TA Utrecht, The Netherlands

^b Wageningen UR Glastuinbouw, P.O. Box 644, 6700 AP Wageningen, The Netherlands

^c Aquamarijn, Berkelkade 11, 7201 JE Zutphen, The Netherlands

^d Nuon-Helianthos, Westervoortsedijk 71, P.O. Box 2134, 6802 CC Arnhem, The Netherlands

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ABSTRACT

We present a novel method to achieve light trapping in thin film silicon solar cells. Unlike the commonly used surface textures, such as Asahi U-type TCO, that rely on light scattering phenomena, we employ embossed periodically arranged micro-pyramidal structures with feature sizes much larger than the wavelength of visible light. Angular resolved transmission of light through these substrates indeed showed diffraction patterns, unlike in the case of Asahi U-type substrates, which show angular resolved scattering. Single junction amorphous silicon (a-Si) solar cells made at 125 °C on the embossed structured polycarbonate (PC) substrates showed an increase in current density by 24% compared to a similar solar cell on a flat substrate. The band gap and thickness of the i-layer made by VHF PECVD are 1.9 eV and 270 nm respectively. A double p-layer (nc-Si:H/a-Si:H) was used to make proper contact with ZnO:Al TCO.

Numerical modeling, called DokterDEP was performed to fit the dark and light current–voltage parameters and understand the characteristics of the cell. The output parameters from the modeling suggest that the cells have excellent built-in potential (V_{bi}). However, a rather high recombination voltage, V_{rb} , affects the FF and short circuit current density (J_{sc}) for the cells on Asahi as well as for the cells on PC. A rather high parallel resistance $\gg 1 \text{ M}\Omega \text{ cm}^2$ (obtained from the modeling) infers that there is no significant shunt leakage, which is often observed for solar cells made at low temperatures on rough substrates. An efficiency of more than 6% for a cell on PC shows enormous potential of this type of light trapping structures.

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1. Introduction

Fabrication of thin film silicon solar cells on low-cost plastics is a challenge for researchers due to the temperature limitation that the substrate imposes, which not only poses difficulty in depositing the right kind of silicon layers, but also to construct the right kind of light confinement structure. Such devices require deposition processes at temperatures near 100 °C where a standard plasma enhanced chemical vapor deposition (PECVD) of hydrogenated amorphous silicon (a-Si:H) usually leads to increased structural disorder and defects in the material [1]. Moreover, textured $\text{SnO}_2\text{:F}$, widely used in superstrate solar cell structures [2], and rough silver [3], widely used in substrate type of cells, are ruled out due to temperature limitation of the substrates whose glass transition temperatures are typically around 100 °C. $\text{SnO}_2\text{:F}$ type of transparent conductive oxide (TCO) for solar cells on plastics is possible to use only in transfer/lift-off methods such as in

Helianthos concept [4]. Inclusion of Al in sputtered Ag for substrate type of cells allows to bring down the processing temperature of textured Ag to below 300 °C [5] from the usual ~350–400 °C used for pure Ag [3]. Using Al doped Ag reflectors Fuji Electric has been able to make thin film silicon solar cells on high temperature resistant plastics (polyimide) in a roll to roll process [6], however, the processing temperature is still too high for cheap plastics such as polyethylene terephthalate (PET), polyethylene naphthalate (PEN) or polycarbonate (PC). Texture etching with diluted HCl of sputter deposited ZnO:Al on plastics has allowed such substrates in combination with conformal coating of thin Ag layer to be used as back reflector in n–i–p solar cells [6]. One of the issues is that the substrate suffers from heavy stress due to the ZnO:Al sputter deposition. Even a reduction of power and an increase of pressure leave the foil with substantial stress. It is also interesting to note that, solar cells on cheap plastics such as PET in p–i–n superstrate configuration have been reported only on flat TCO (ZnO:Al) substrates [7] with very low efficiency (~3%); most of the solar cells on plastics (PET or PEN) have been made in n–i–p configuration [8–11]. The difficulty in making textured features on TCO is speculated to be one of the reasons for this failure to make p–i–n cells on cheap plastics.

* Corresponding author. Tel.: +31 30 2532961; fax: +31 30 2543165.

E-mail address: J.K.Rath@uu.nl (J.K. Rath).

In this paper, we have used an alternative approach, namely fabrication of superstrate type amorphous silicon solar cells on conformally TCO coated micro-pyramidal textured plastic (PC) substrates.

2. Experimental

2.1. Depositions

Depositions of all the intrinsic silicon thin films (Table 1) for solar cells were made by very high frequency plasma enhanced chemical vapor deposition (VHF PECVD) at a frequency of 60 MHz, using a shower head electrode reactor, in an ultra high vacuum multichamber deposition system called ASTER [12]. The doped layers were also made in the ASTER system at a VHF of 50 MHz. The substrate temperature was controlled by the set temperature of the heater. ZnO:Al was deposited by a magnetron sputtering system called Salsa [13] from a ZnO:0.5% Al₂O₃ target for the front contact and ZnO:2% Al₂O₃ target for the back reflector, whereas the metal layers (Ag and Al) were deposited by thermal evaporation. Thickness and optical properties (band gap, absorption coefficient, etc.) were obtained by modeling reflection/transmittance measurements fitted to the OJL model [15].

Single junction p–i–n cells were made with thin film silicon p, i and n layers deposited at 125 °C followed by a ZnO:Al/Ag/Al back reflector. The completed cells were annealed for 1 h at 125 °C in a nitrogen atmosphere, after which current voltage (I–V) measurements were done in the dark and under calibrated AM1.5 100 mW/cm² light of a dual beam solar simulator (WACOM, Japan) at 25 °C and spectral response measurements were done to obtain the external collection efficiency (ECE).

3. Results

3.1. Textured substrate

Before fabricating the textured substrates, simple optical modeling was done to understand the scope of textured substrates for light trapping. Normally, for thin film solar cells, random textures of very low dimensions with scattering properties are used [13]. The analysis of the optical effects of those features is very complex. In the present case, we employ large features, i.e., feature sizes much larger than the effective wavelength of light. This allows for simple ray tracing techniques to model the optical effects and light trapping phenomena. Such a modeling on a structure; air/glass/TCO/amorphous silicon/air, with light entering from air onto the glass was done to simulate the situation of a solar cell. The modeling indeed showed that there is a light trapping effect in the silicon layer when there is a pyramidal feature facing the silicon layer. The light trapping effect (absorption) increased monotonously with increasing the pyramidal angle (the angle between faces of pyramid and the base), reaching a maximum around an angle of 40–45°. Details of this optical modeling are published elsewhere [14]. The textured surface features on PC used in this study are similar to the optimal features according to the simulation. The textured micro-pyramidal surface was made on one side of the PC substrate by hot embossing, whereas the other side is kept flat. For the hot embossing, first a suitable master, which is in our case a nickel master, is made. The master is

Table 1

Light I–V characteristics of the a-Si cell on embossed polycarbonate, flat glass and Asahi U-type substrates. R_{sc}: resistance at the short circuit current, R_{oc}: resistance at the open circuit voltage. The error in current density is within ± 1.5%.

| a-Si cell on substrate | V _{oc} (V) | J _{sc} (mA/cm ²) | FF (%) | η (%) | R _{sc} (kΩ cm ²) | R _{oc} (Ω cm ²) |
|------------------------|---------------------|---------------------------------------|--------|------------|---------------------------------------|--------------------------------------|
| PC-pyramid | 0.87 ± 0.01 | 12.33 ± 0.15 | 0.59 | 6.36 ± 0.1 | 0.85 ± 0.03 | 9.6 ± 0.3 |
| Asahi-U | 0.93 ± 0.01 | 12.82 ± 0.15 | 0.64 | 7.54 ± 0.1 | 1.24 ± 0.04 | 9.4 ± 0.3 |
| Glass | 0.93 ± 0.01 | 9.50 ± 0.15 | 0.64 | 5.9 ± 0.1 | 1.19 ± 0.04 | 7.5 ± 0.3 |

pressed against the PC substrate which is heated up and the structure is transferred onto the plastic. For deciding on the feature sizes to be embossed, we consider that the light trapping effect is due to geometric effects in the solar cell. Therefore the feature size is not important as long as it is larger than the wavelength of light. Fig. 1 shows a SEM image of an embossed PC substrate. Regularly arranged micro pyramidal features of 10 μm lateral size are observed. Angular dependence of the transmitted light (measured with a 632.8 nm HeNe laser, light entering from the flat surface) from these pyramidal textured substrates showed only sharp interference peaks (Fig. 2), unlike the angular resolved scattering (ARS) that one observes for conventional textured TCO substrates, such as Asahi U-type SnO₂:F coated glass [13].

3.2. Solar cells

Device quality a-Si:H films with a photosensitivity of ~10⁵ were made at 125 °C with a hydrogen dilution, H₂/SiH₄, of 5. Moreover, p-type a-Si and nanocrystalline silicon (nc-Si) and n-type a-Si films were also developed for a substrate temperature of 125 °C. The ZnO:Al TCO layers and the metal layers were made below 100 °C. With these materials solar cells were made with the following structures:

- (Asahi U-type TCO substrate): glass/SnO₂:F/p a-Si:H/i a-Si:H/n a-Si:H/ZnO:Al/Ag/Al
- (Flat substrate): glass/ZnO:Al/p-nc-Si:H/p a-Si:H/i a-Si:H/n a-Si:H/ZnO:Al/Ag/Al
- (PC micro-pyramidal substrate): micro-pyramid PC/ZnO:Al/p nc-Si:H/p a-Si:H/i a-Si:H/n a-Si:H/ZnO:Al/Ag/Al.

The sheet resistance of the ZnO:Al TCO (front contact) is 14 ± 1 Ω/sq (ZnO:Al 0.5% 1 micrometer thick), whereas the sheet resistance of the Asahi TCO is 10 ± 1 Ω/sq. The area of the cells was 0.16 cm². The thickness of the i-layer was confirmed from cross-sectional transmission electron microscopy (XTEM) image of the cells to be 270 ± 10 nm.

The solar cell on ZnO:Al coated substrates needed a double p-layer for a proper electrical contact of the ZnO:Al with the p-layer. A Wacom dual beam solar simulator in combination with a Keithley 238 voltage source/current measure unit is used to perform I–V measurements on completed cells. The spectrum is calibrated to the AM1.5 spectrum through NREL calibrated reference cells within 3%. The accuracy in voltage is determined by the step size of 0.01 V. Fig. 3 shows the comparison of the I–V characteristics of the solar cell on PC (cell #3) with the cell on a flat glass substrate (cell #2) and a cell on Asahi U-type TCO glass; both the cell on PC and cell on glass use ZnO:Al as the front contact. The open circuit voltage (V_{oc}) of the cells on the flat substrate and on the Asahi TCO reaches a

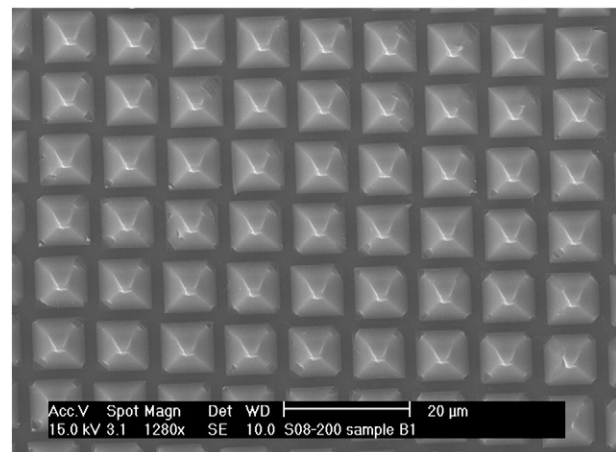


Fig. 1. SEM image of the micro-pyramidal embossed structures on a PC substrate used in this study.

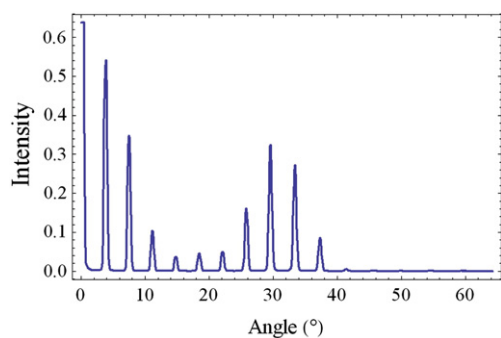


Fig. 2. Angular dependent transmittance of a substrate as shown in Fig. 1. The light (632.8 nm HeNe laser) enters through the flat side of the PC.

high value of 0.93 ± 0.01 V. This high voltage is attributed to the high band gap value (1.9 eV) of the i-layer. The voltage is slightly lower for the cell on PC, attributed to a higher dark current. However, the enhancement in short circuit current density (J_{sc}) by 24% of the PC cell compared to the cell on flat glass, due to light trapping in the cell on a pyramidal textured PC, is very promising. The spectral response (Fig. 4) clearly shows this enhancement. The question that now arises is whether the cell performance on textured PC is better than that on Asahi TCO (cell #1). Table 1 gives the solar cell parameters of these two types of cells. The efficiency of the cell on textured PC is $6.4 \pm 0.1\%$, which is just $\sim 1\%$ absolute lower in efficiency compared to the cell on Asahi TCO.

The main difference between the cells on Asahi TCO and PC lies in the FF and V_{oc} . The spectral response of the cell on PC is compared with that on Asahi TCO, as shown in Fig. 4. In the red part, the ECE of the cell on PC is slightly lower around 600 nm. However, the major difference is observed below 500 nm. From a comparison of the spectral response under short circuit conditions and under reverse bias we see only a marginal increase in current at reverse bias for both the cells on Asahi and on polycarbonate, ruling out any barrier at the ZnO/p<nc> to be the cause for the spectral response behavior at low wavelength region. The lower J_{sc} of the cells is primarily due to a lower spectral response in the blue region, which is attributed to the lower band gap of the ZnO:Al TCO (used in these cells) compared to that of Asahi TCO (SnO₂:F). Optical studies, presented in Fig. 5, revealed that the transmittance (T) of the ZnO:Al layers, used as front contact in these cells, decreases substantially below 450 nm, from $T > 80\%$ above 500 nm, whereas the Asahi TCO glass shows transmission down to 300 nm. This transmission loss explains

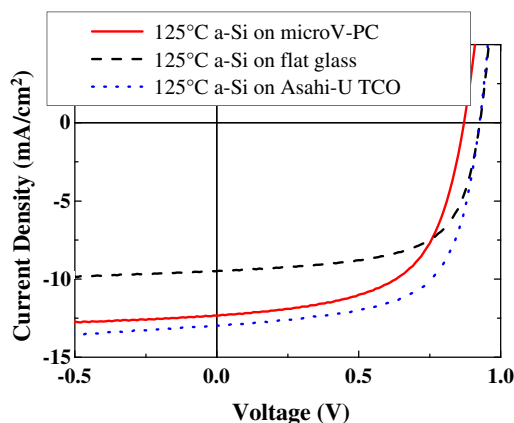


Fig. 3. Measured I–V characteristics of an a-Si solar cell on micro pyramidal textured PC (solid), compared to that on flat glass (dashed) and on Asahi U-type TCO (dotted). Similar ZnO:Al layers are used as front contact for the cell on micro pyramidal textured PC and the cell on flat glass.

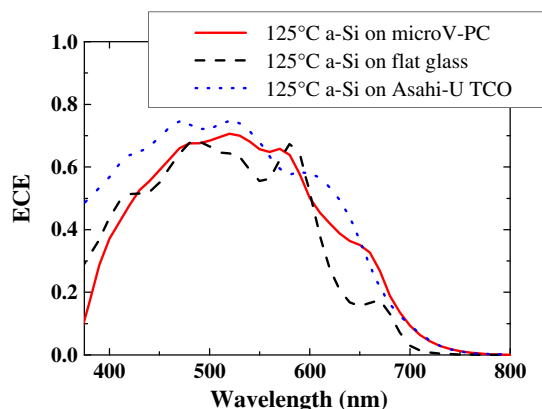


Fig. 4. External collection efficiency of an a-Si solar cell on micro pyramidal textured PC (solid), compared to that on flat glass (dashed) and on Asahi U-type TCO (dotted). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

the lower spectral response in the short wavelength region for the a-Si solar cell on PC, because ZnO:Al is used as front contact in these cells. Also shown is the transmittance of glass and PC without the ZnO:Al TCO layer. Glass shows more transmission in the short wavelength region, even below 300 nm, whereas PC blocks all the light with wavelengths below 380 nm. But, because the ZnO:Al absorbs all light below 350 nm, the difference in transmission between the ZnO:Al coated glass and the ZnO:Al coated PC is very small.

Numerical modeling, using software called DokterDEP developed at Nuon Helianthos b.v., was performed to fit the dark and light current–voltage characteristics and understand the performance of the cells. In this simulation, the bias dependent change of the photocurrent, due to change in the recombination current is modeled [16,17] as,

$$J_{ph}(V) = J_{ph0} * \chi(V) \quad (1)$$

where J_{ph0} is the maximum photocurrent and the function $\chi(V)$ is given by,

$$\chi(V) = \left(\frac{V - V_{bi}}{V_{\mu}} \right) \left(1 - e^{-\frac{V_{\mu}}{V - V_{bi}}} \right) \quad (2)$$

in which $V_{\mu} = d_i / \mu \tau_{eff}$ is the recombination voltage where d_i is the i-layer thickness and $\mu \tau_{eff}$ is the effective mobility–life time product. V_{bi} is the built-in potential. Table 2 shows the output parameters of the simulations done on the cells on Asahi TCO and textured PC.

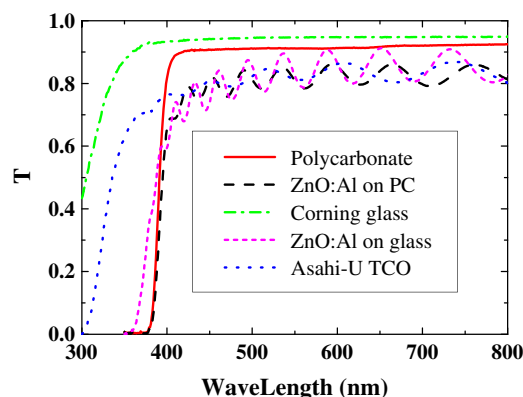


Fig. 5. Total transmittance of different substrate materials: Corning glass, ZnO:Al coated Corning glass, PC, ZnO:Al coated PC and Asahi U-type TCO glass.

Table 2
Output fitting parameters obtained by numerical modeling of the dark and light I–V data. n: diode quality factor, J_0 : saturation current density, R_s : series resistance in vertical stack, R_p : parallel shunt resistance (from dark I–V), J_{pho} : maximum photoconductivity (if all generated current would be collected), V_{bi} (built-in voltage), V_μ (recombination voltage) (from light I–V).

| a-Si cell on substrate | J_0 (mA/cm ²) | n | R_s (Ω cm ²) | J_{pho} (mA/cm ²) | V_{bi} (V) | V_μ (V) |
|------------------------|-----------------------------|---------------|------------------------------------|---------------------------------|----------------|-----------------|
| PC-pyramid | $8 (\pm 2) \times 10^{-8}$ | 2.0 ± 0.1 | 0.8 ± 0.1 | -12.8 ± 0.1 | 0.90 ± 0.1 | 0.15 ± 0.01 |
| Asahi-U | $4 (\pm 1) \times 10^{-10}$ | 1.6 ± 0.1 | 0.8 ± 0.1 | -13.7 ± 0.1 | 0.96 ± 0.1 | 0.12 ± 0.01 |

4. Discussion

Simulation of the I–V characteristics revealed higher recombination of carriers in the i-layer of the cell on PC; this cell has a higher diode quality factor n and saturation current density J_0 (two orders of magnitude higher) compared to the cell on Asahi TCO. This recombination argument is again supported by a high recombination voltage, V_μ , which has a detrimental effect both on FF and J_{sc} . It is of interest to note that the built-in potential V_{bi} is very high for both cells, though the cell on Asahi TCO has slightly higher built-in potential. This manifests in a higher V_{oc} for cells on Asahi TCO. The maximum generated photocurrent (purely the optical effect, without recombination), J_{pho} , is only ~ 1 mA/cm² smaller in case of the textured PC substrate compared to the Asahi U-type substrate.

It is not straightforward to understand why the cell on PC should have more recombination than the one on Asahi TCO. As the deposition conditions used for these cells are the same (made in the same run), it is not expected that there is any substantial difference in the gas phase process. The change of temperature of the substrate during the a-Si:H deposition was also considered and it was found by measurement with a thermocouple that under the deposition conditions used in this study, a temperature rise of not more than 3 °C occurs. Residual gas analysis also did not reveal any measurable degassing from the PC substrate. Hence, we may speculate that due to substrate morphology induced structural evolution, the defect density is higher in the i-layer of the solar cells on PC [18].

XTEM images indeed show cracks in the silicon layers in cells on PC. An example is shown in Fig. 6. It is still an open question whether the cracks are caused by the morphology of the substrate or by the extrinsic stress due to differences in thermal expansion coefficients between the substrate and the layers. Earlier reports on a-Si cell made on textured TCO on flexible metal foil substrates showed such defects in the a-Si layer [19] whereas the same layer on similar textured TCO on glass did not show any defects. Normally, cracks tend to be present near sharp valleys in the TCO/silicon interface. In the present study, as we have no sharp valleys (there is some flat area between the pyramids), we expect our cracks not to be caused by the morphology. Further research is however needed to determine the exact cause of these defects and find solutions.

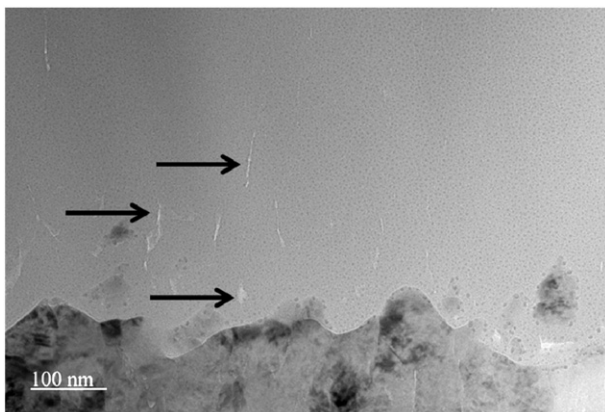


Fig. 6. XTEM image of an amorphous silicon solar cell deposited on a polycarbonate substrate. Small cracks are visible in the a-Si, which are indicated by the black arrows.

The next question is; how do the features much larger in size than wavelength of light contribute to light trapping. The numerically simulated short circuit currents in a thin film silicon cell, using a modeling based on Maxwell's equation, shows that the current goes up with increase of feature periods, however, for feature periods above 1 μ m the current drops almost to the value of flat cell [20]. On the other hand, if the diffraction angle from the periodic structure is larger than the angle of total reflection in the solar cell, the light from this diffraction order will be trapped within the device [21]. But for our large pyramid spacing, we only expect a small contribution for this effect. Also, because the film thickness is small compared to the pyramid spacing, the diffraction effect is only expected to play a minor role. Ray tracing studies show that the gain in absorption of the light is caused by the angle of the TCO–silicon interface with respect to the incoming light. If the pyramid angle is right, light will be trapped inside the silicon by total internal reflection. A reflection study confirms a reduction in the reflectance (measured from the front side of the cell) of the cell on micro pyramidal textured PC compared to that of the cell on flat glass, as shown in Fig. 7. Moreover, one needs to understand that the photon management consists in effectively localizing light [22] in the absorbing layer of the solar cell. Further work is needed to understand how the light is localized inside the i-layer of the cell made on the large pyramidal features.

5. Conclusion

Amorphous silicon solar cells on embossed micro-pyramidal textured PC substrates yielded $6.4 \pm 0.1\%$ initial efficiency. The light trapping due to pyramidal surfaces was achieved by pure geometric effects, as the feature sizes are much larger than the effective wavelength of light in the cell and are not expected to cause scattering of light. Detailed numerical modeling showed that the cells on textured PC do have enough room for improvement if the recombination current in the cells can be reduced. The high band gap of the intrinsic a-Si:H layers made at low temperature lifts the open circuit voltage to high values, reaching near 1 V for the cell on a flat surface. The study shows that a substantial light trapping is possible by a simple geometric effect, such as multiple reflection inside the cell, for which embossed features with an appropriate angle ($\sim 45^\circ$) to the substrate surface, as predicted by simulation, are needed. In this study we showed that pyramidal features, even of 10 μ m size, show encouraging light trapping effect.

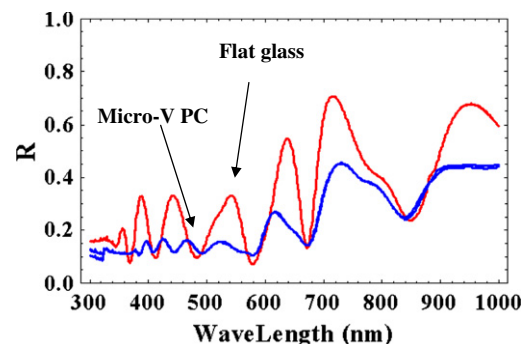


Fig. 7. Reflectance of the cells on micro pyramidal textured PC and flat glass, when measured with light falling on the front side (flat side of the substrate) of the cell.

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