Anisotropic Etching of Three-Dimensional Shapes in Silicon

The Important Role of Galvanic Interaction

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As a result of the exposure to solution of different crystallographic facets during anisotropic etching of three-dimensional structures in silicon, the open-circuit potential of the semiconductor can change markedly. Using a (100)Si substrate, masked to reveal (111) facets, we show that such a shift in potential can alter the chemical etch rates of the individual facets. The extent of the changes depends both on the facets exposed and on their relative areas. Because the surface geometry, and with it the silicon potential, change continuously in time, chemical etching must adapt continuously to these changes. This is an interesting example of a self-regulating system with a complex feedback mechanism. The effects described in this work clearly influence anisotropic etching ratios and are therefore important for the fabrication of microelectromechanical systems.
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Anisotropic etching of silicon in alkaline solutions is an important step in the technology of microelectromechanical systems (MEMS).[1] Etching is employed to make high-definition, three-dimensional structures in silicon wafers. These are required for a range of applications including miniature sensors for the measurement of pressure, flow, angular rate, and velocity. Other microsystems, such as filters, resonators, valves, pumps, and optomechanical connectors, can also be fabricated. The form that is obtained depends on the surface orientation of the wafer, the mask geometry, and the relative dissolution rates of the various crystallographic faces exposed during etching. The low etch rate of the (111) face with respect to that of other faces is exploited to produce deep grooves with flat walls, inverted pyramids, V-shaped grooves, and various other forms.[1-3] For (100)-oriented wafers, widely used in MEMS technology, the ratio of the etch rates of (111) and (100) faces, referred to here as the anisotropic ratio, is of vital importance for making high-resolution micromechanical structures. Although in the most favorable case the anisotropic ratio can exceed 100,[4] control and reproducibility at this level are poor. The composition of the etchant and the etching conditions as well as the (mis)orientation of both the wafer surface and the mask edge are clearly important. Other factors which may play a role are dislocations in the silicon, defects at the silicon-mask interface, and impurities (even at very low concentrations) in the etchant.[4]

Because of the practical importance of etching anisotropy, extensive studies have been devoted to mapping the etch rates of the various crystallographic faces of silicon in different alkaline etchants. Two experimental approaches have been used. In the first, a silicon sphere or a hemispherical cavity with a diameter of some millimeters is etched; anisotropy gives rise to facetting which, in turn, gives information about the (relative) etch rates of different crystal planes.[5-7] In the second approach, a silicon wafer is masked with, for example, silicon nitride, and the semiconductor is etched through the windows in the mask. Because the mask has a characteristic "wagon wheel" shape, many crystallographic faces are addressed in a single experiment.[8,9] Both methods yield two-dimensional contour maps showing lines of constant etch rate as a function of crystallographic direction. Such maps have proved invaluable in interpreting three-dimensional shapes etched in masked wafers. In addition to this experimental approach, theoretical models have been developed with the aim of understanding etching mechanisms and explaining the contour maps.[10-12]

Anisotropic etching of silicon in alkaline solutions is considered a predominantly chemical process, *i.e.*, the various steps of the dissolution reaction involve only a local exchange of electrons between Si-Si surface bonds and the etching agent (H$_2$O).[13-16] That etching is chemical is clear from the fact that *p*-type silicon continues to dissolve at a high rate at negative potentials.[17,18] Under such conditions, electrochemical or electroless dissolution involving free charge carriers cannot occur.[19]

Besides chemical etching, silicon can also undergo electrochemical oxidation in a reaction which gives rise to a current (anodic) in the external circuit (see below).[13-16,20] The dissolution rate resulting from this process is much lower than that from chemical etching. In addition, electrochemical reduction of water (and dissolved oxygen) can occur. The rates of these oxidation and reduction reactions determine the open-circuit potential (OCP) of the etching silicon. (At open-circuit, the anodic and cathodic currents must be equal.) The OCP for a given etchant depends on the crystallographic orientation of the wafer, being more positive for (111) than for (100) surfaces.[21,22]

Although anisotropic etching is a chemical reaction, it has been shown that the etch rate can in certain cases be influenced by an applied potential. For example, etching of *n*-type (100) silicon is either partly or completely suppressed at potentials negative of the OCP; this is not the case for *p*-type (100) silicon.[17,18] A similar strong reduction in etch rate has been observed for n-type (111) silicon[17,20] and a less pronounced effect was noted for the *p*-type (111) material.[17]

In the course of an anisotropic etching experiment, different crystallographic facets become exposed to the solution and the areas of the facets change as a function of etching time. Because each face contributes to the total electrochemistry of the system, the OCP will depend on both the faces exposed and their relative areas. The system acts as a galvanic cell, as has been shown previously for electroless etching of GaAs.[23] The importance of such galvanic effects in silicon etching has been pointed out by Allongue and coworkers;[24,25] they showed that cathodic protection of a polished (111) surface by a roughened back surface in oxygen-free NH$_4$F solution helps to obtain ideally flat hydride-terminated (111) surfaces. Considering the discussion above one might expect the anisotropic etching characteristics (*e.g.*, the anisotropic ratio) to depend on the particular "facet geometry" which, of course, should be time-dependent. In this work we show, on the basis of electrochemical and etching experiments, that this is indeed the case. Such effects can play a key role in anisotropic etching.

Experimental

Experiments were carried out on an *n*$^+$-type (100)Si wafer (arsenic-doped, 0.01 ohm.cm) and on standard *n*-type and *p*-type (100) wafers (1-30 ohm.cm), provided with an Ohmic contact, and masked with Si$_3$N$_4$ in such a way that V-shaped grooves arise during etching. The principle of our approach is shown in Fig. 1 for a single
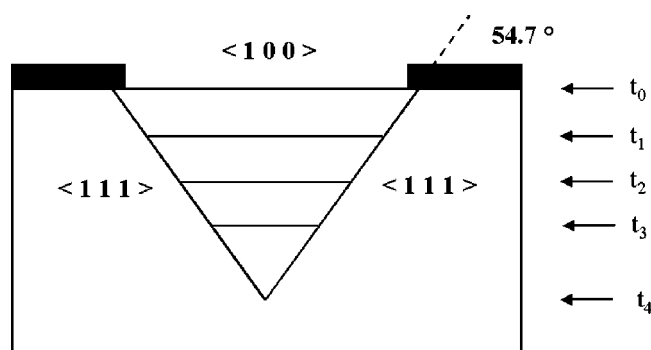
Figure 1. Schematic representation of the electrode geometry. One groove from an array of grooves is shown. The (100) surface of the silicon is masked in such a way that (111) facets are revealed during etching. As a result, the area of the (100) surface decreases while that of the (111) surface increases in time. The figure shows a number of stages in this process, including the final V-groove.

Figure 2. I-U curves for a masked *n*-type silicon electrode in aqueous 33% KOH solution at 80°C measured after various etching times. The voltage was scanned from negative to positive at a rate of 10 mV/s. Initially ($t = 0$ min), only the (100) surface is exposed to solution. The second scan was made after 10 min and subsequent scans at 15 min intervals up to 190 min. In the final scans only the (111) surface is exposed. The change in open-circuit potential ΔU_{OC} on going from the (100) to the (111) surface is also indicated.

groove. This can be made by aligning the opening in the silicon nitride mask along the (110) direction on the (100) wafer. Chemical etching exposes slow-etching (111) planes under the resist edge, giving rise to a groove that ultimately acquires a V-form. As etching proceeds, the area ratio of the (100) to the (111) faces obviously decreases. The actual electrode did not consist of a single groove but of an array of grooves. The groove width (140 µm) is typical of that required for making optical fiber guides.

The masked silicon wafer formed the working electrode in a two-electrode electrochemical cell which contained the anisotropic etchant. Platinum was used both as a counter and a quasi-reference electrode. At various times during the development of the grooves the current density was recorded as a function of the potential in a sweep experiment from negative to positive potentials. The sweep rate was 10 mV/s. In another series of experiments the wafer was removed from solution at various times to measure the etched depth and the degree of underetching, which are determined by the (100) and (111) etch rates, respectively. For the determination of the etched depth the stylus of a calibrated Dektak 3030 profilometer was traced along a line perpendicular to the groove direction. An optical microscope (Reichert-Jung Polyvar) equipped with a Polyspec photometer was used to investigate the groove structure; by adjusting the focal plane we could measure the width at the bottom and top of the groove. Underetching was studied by determining the undercut of the nitride mask using the microscope (the undercut was on the order of 1 µm and could be measured with a resolution better than 0.1 µm). The area of the (111) surface exposed to solution could be calculated from the tilt of the (111) plane, the total groove length and the etched depth. The deviation of the (111) face from the ideal angle of 54.7° was below 1°. The dimensions of the base of the groove yielded the (100) area. All experiments were performed in an aqueous 33% KOH solution at 80°C.

Results

Figure 2 shows the results of current-potential (I-U) measurements on an n-type electrode. In the first scan ((100) surface), a broad anodic peak due to electrochemical oxidation of silicon is observed; this is as expected for a (100) face in KOH solution.[14,15,18,22] Passivation occurs at higher potential. At negative potentials a cathodic current results from electrochemical reduction of water to hydrogen. The anodic and cathodic processes determine the open-circuit potential (-1.3 V) of the system.

As the grooves are formed, the peak current decreases and the maximum shifts to negative potential. Because this is a two-electrode experiment and the maximum current is not negligible, both the form of the peak and the peak potential will be determined to some extent by Ohmic loss. It is clear that a second peak gradually develops at more positive potentials; this is due to a contribu-
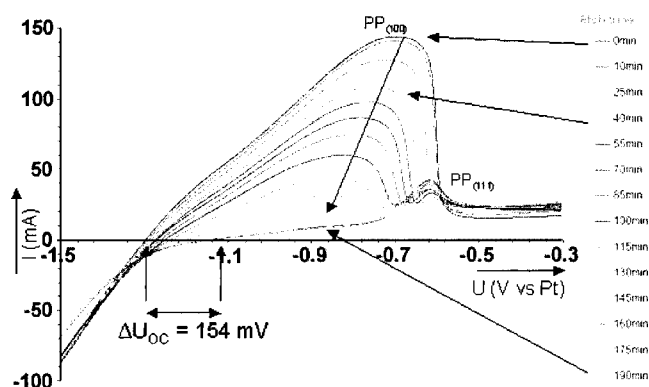
tion from the (111) side walls of the grooves. Eventually, after the V-grooves are fully formed, only the peak due to the (111) face is found. The anodic peak current for the (111) surface is considerably smaller than that for the (100) surface; clearly, it is easier to passivate the (111) face.[17,22] An important feature of the results in Fig. 2 is the considerable positive shift in the OCP of the system ($\Delta U_{OC} > 150$ mV) as the surface changes from a (100) to a (111) orientation (Fig. 3). This result agrees with the idea that the (111) surface is more "noble" than the (100) surface.

Smith *et al.*[22] used a similar V-groove approach to produce well-defined (111) surfaces in silicon. Their current-potential curves for the initial state (the (100) surface) and the final state (the (111) surface) show the same trends as observed here, although the experimental conditions were somewhat different (40% KOH solution, 60°C). As in our case, the OCP of the (111) facetted n-type electrode was more positive (160 mV) than that of their initial (100) electrode; the difference for the p-type electrode was even larger (270 mV).

The etched depth (*i.e.*, in the (100) direction) and the degree of underetching were measured after 60, 105, and 150 min. From these values the etch rate of the (100) face and the underetch rate were determined for each of the three periods. The etch rate was calcu-
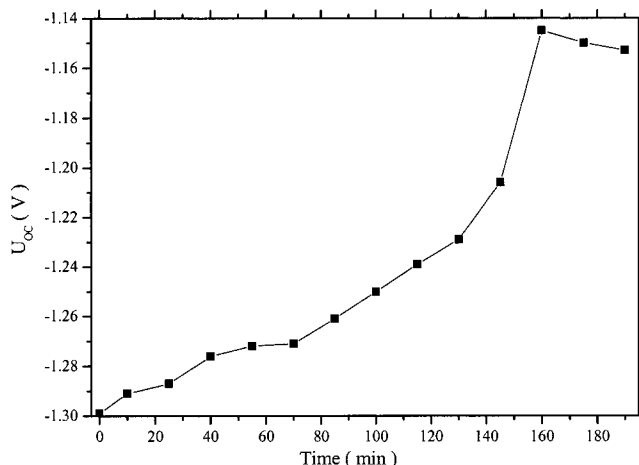

Figure 3. The time-dependence of the open-circuit potential of *n*-type silicon corresponding to the transition from the (100) to the (111) surface (see Fig. 2).
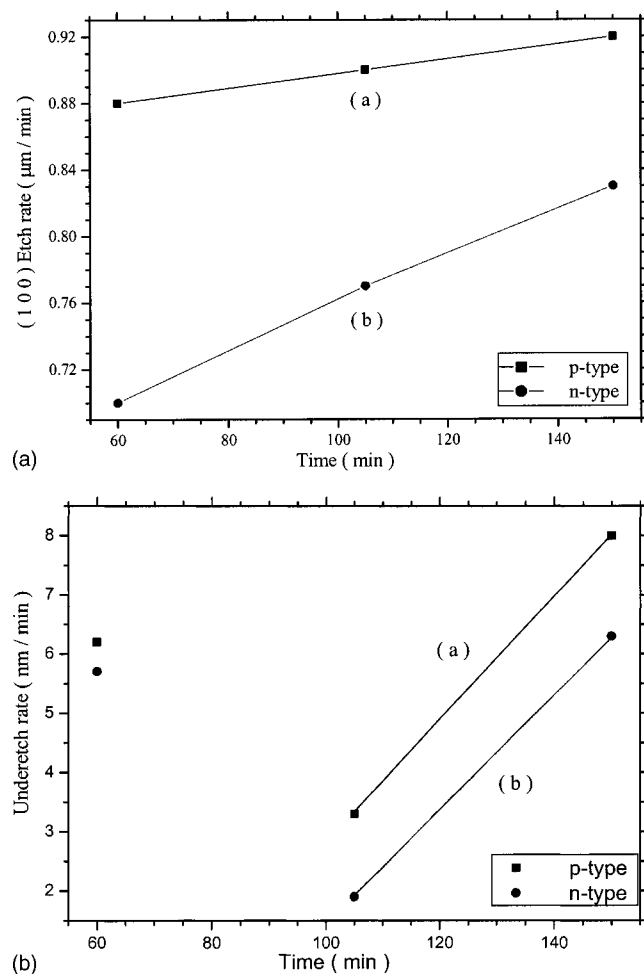
(a)

(b)

Figure 4. (a) The average (100) etch rate of (a) *p*-type and (b) *n*-type silicon measured for three periods during V-groove development. (b) The average underetch rate of (a) *p*-type and (b) *n*-type silicon for the same experiment.

lated from the profile at the beginning and end of the period (*e.g.*, 105 and 150 min, for the third period). From Fig. 4a, curve (a) it is clear that the (100) etch rate of the *p*-type sample changes very little during the course of etching as the area ratio of the (100)/(111) faces decreases to a low value (the area ratio is shown in curve (a) of Fig. 5 for the three etch times). The etch rate of the *n*-type sample (Fig. 4a, curve (b)), however, increases by almost 20% in the same period. The change in area ratio for this case is given in curve (b) of Fig. 5. Figure 4b shows corresponding results for the underetching. Here, the etch rate of both *n*-type and *p*-type samples is "high" for the first period and then drops considerably in the second period. The initial high etch rate is due to the difficulty of aligning the mask edge perfectly along the desired crystallographic orientation. A slight misalignment of the mask can give a higher underetch rate. The etch rate drops as the etching face becomes aligned. A comparison of the results in Fig. 4a and b shows that in the second period the ratio of the vertical (100) and underetch rates is extremely high (almost 300 for the *p*-type and 400 for the *n*-type wafers). In the third period the underetch rate for both types of silicon shows a significant increase, the relative increase being more marked for *n*-type than for *p*-type silicon. The corresponding change in area ratios is shown in Fig. 5.

Discussion

The etching results shown in Fig. 4 can be understood on the basis of the electrochemistry of these systems (Fig. 2) and previous results of the potential dependence of the chemical etch
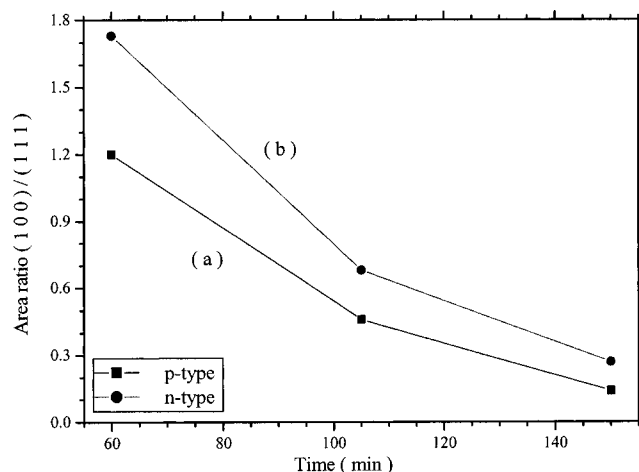

Figure 5. The time-dependence of the area ratio of the (100) and (111) surfaces corresponding to the experiments of Fig. 4.

rates.[13,18,20,23] Electrochemical measurements at high temperature and KOH concentration have shown that the etch rate of *p*-type (100) silicon does not depend on the applied potential in the vicinity of the open-circuit value.[18] On the other hand, the etch rate of *n*-type silicon was found to increase as the applied potential is made positive with respect to the open-circuit value.[18] The etching of V-grooves involves a positive change of the OCP of the system as the (111) surface takes over from the (100) surface (Fig. 3). This has little effect on *p*-type silicon but leads to a significant increase in the etch rate of *n*-type silicon. The difference in potential dependence of the two types of material is due to the nature of the space-charge layer at the silicon/solution interface.[18,20] Under etching conditions the *n*-type semiconductor is in accumulation and, as a result, the potential drop across the Helmholtz layer changes when the silicon potential is changed. This can influence the rates of the individual steps of the chemical etching reaction.[13,18,20] The extent of the increase in the open-circuit etch rate of *n*-type (100) silicon observed in the present experiments (Fig. 4, curve (b)) agrees with previous work[18] in which the silicon potential was fixed by an external source. Under etching conditions *p*-type silicon is in depletion and, consequently, the Helmholtz potential does not change with applied potential. As a result, the chemical etch rate is essentially independent of potential.

There are no results available on the influence of potential on the chemical etching of (111) Si under conditions similar to those used in the present work (high KOH concentration, high temperature). Experiments performed by Glembocki *et al.* with 2M KOH at 20°C showed that, as for *n*-type (100) Si at low KOH concentration,[17] etching of *n*-type (111) Si can be completely suppressed at negative potentials. The etch rate shows a maximum at the OCP. The etch rate of *p*-type (111) Si was also found to decrease, but less drastically, with decreasing potential.[17] These experiments likely did not involve perfect (111) surfaces which are difficult to obtain and impossible to maintain during macroscopic etching experiments. Allongue and coworkers used *in situ* scanning tunneling microscopy to study etching of *n*-type (111) Si in 2 M NaOH solution at room temperature.[20] They showed that etching proceeds by a step-flow mechanism involving attack on the edges of (111) terraces. As the potential is made positive, approaching the open-circuit value, considerable roughening of the step edges is observed, as well as the formation of etch pits on the flat (111) terraces.[20,26] From the rate of retraction of the step edges, the etch rate could be determined. Allongue *et al.* found etch rates comparable to those reported by Glembocki *et al.*[17] for *n*-type (111) Si and a similar potential dependence. Allongue and coworkers were the first to attribute the suppression of etching of *n*-type Si to electron accumulation at the surface.[20] Such an explanation is compatible with a weaker potential

dependence in the case of *p*-type (111) Si. If we assume that these results, obtained under mild conditions, can be extrapolated to high temperature and high OH⁻ concentration, then the trend in underetch rate can be understood. Ignoring the initial "high" etch rate due to mask effects, we see in Fig. 4b that the underetch rate increases as the surface evolves from (100) to (111), *i.e.*, as the potential approaches the open-circuit value for the (111) surface.

These results show that profile etching of silicon in alkaline solution may act as a self-regulating system. Chemical etching exposes various faces to solution; their areas change in time. As a result, the OCP of the system shifts from the value corresponding to the initial surface and this leads to a readjustment of the original etch rates. This feedback mechanism is, in fact, even more complicated. The anodic reaction which, together with the cathodic reaction, decides the OCP is itself determined by chemical etching. It has been shown that electrochemical oxidation of silicon is due to injection of electrons into the conduction band from intermediates of the chemical dissolution reaction.[14] Such effects will clearly influence the general anisotropy of the etching system so that re-examination of previous results in the light of the present work seems desirable.

It is interesting to note that Raisch *et al.* have also used an explanation based on galvanic interaction between (100) and (111) faces to explain the stability of micropyramids formed on (100) silicon during anisotropic etching.[27] The results reported in this paper support their interpretation. A similar effect may also be responsible for the absence of micropyramids in (100) surfaces adjacent to (111) faces during anisotropic etching;[28] micropyramids do not survive at the OCP of (111) Si.

Conclusions

This work shows that local cell formation arising from exposure to solution of different crystallographic faces of silicon may markedly influence anisotropic etching ratios. The magnitude of the effect depends on the semiconductor doping type, on the facets revealed, on the relative areas of these facets, and on the etching solution. The individual etch rates may change considerably in time during an etching experiment. It may, therefore, be instructive to reexamine anisotropy in the light of the present results. Apparent instabilities in orientation-dependent etch rates observed by Frühauf and Hannemann in experiments with wagon-wheel masked samples,[29,30] may be due to galvanic effects. For high reliability and reproducibility in device etching, design rules, which take into account galvanic effects, are required.

The results shown in Fig. 4 and 5 suggest that in certain cases anisotropy could be optimized by fixing the potential of the etching silicon. Very high anisotropic ratios can be obtained. Obviously, the use of an external source may not be so attractive for this purpose, because it requires electrical contacts to the wafer. It should, however, also be possible to regulate the potential without an external source. For example, the OCP of a (100) wafer may be "pinned" at the rather negative value corresponding to (100) Si by exposing to solution a "sacrificial" area of the surface which is relatively large compared to the area being etched for the device. For example, the back of the wafer might be used for this purpose.

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