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Hot Wire Chemical Vapor Deposition: Recent Progress, Present State of the Art and Competitive Opportunities

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Hot Wire CVD (also called Catalytic CVD or initiated CVD) is an elegant low pressure deposition technique for the deposition of functional films, both inorganic and organic, based on the decomposition of precursor sources at a heated metallic surface. The conformal deposition of thin films on rigid substrates or flexible foil substrates, whether in-line or batch type, is very straightforward, since it is plasma-free (i.e. without the risk of a damaging bombardment of energetic ions) and it is easily scalable. An increasing variety of thin film materials can be obtained with this method, with good feedstock gas utilization and high deposition rate. Progress has been made in establishing stable and reproducible conditions for the hot catalytic wires used for efficient decomposition of the source gases. In this paper we discuss some of the current research issues in this field.

Introduction to Hot Wire Chemical Vapor Deposition

Since the first patent in 1979 [1], the Hot-Wire Chemical Vapor Deposition (HWCVD) technique has been improved considerably and presently is a viable method for the deposition of many different functional materials, both organic (polymers) and inorganic. In particular, high quality silicon-based thin films and solar cells can now be made [2-5]. The HWCVD technique can be viewed as a “remote decomposition” technique, since it is based on the decomposition of silicon-containing gasses at a catalytic hot surface, while the substrate itself has no active role in generating the active precursors, unlike the case of PECVD where it usually has a role as the grounded electrode, helping to sustain a homogenous rf field. The absence of the requirement to achieve an equipotential plane at the substrate makes it easier to transport either rigid or foil-type substrate materials during deposition and to scale up to large areas.

Since source gases are catalytically decomposed, the method is sometimes also referred to as thermo-catalytic CVD (TCCVD) [6] or catalytic CVD (Cat-CVD) [7]. The technique is also known under the abbreviations HFCVD and iCVD. The term Hot Filament CVD (HFCVD) is the oldest and normally used in the field of deposition of diamond and other carbon-containing layers. The term i-CVD is the newest and is used to describe polymer deposition using initiator molecules and monomer precursors. HWCVD and Cat-CVD are mutually exchangeable terms for the process of depositing (mainly) inorganic thin films in general.

Usually, tungsten or tantalum filaments are used as catalyst, with filament temperatures roughly between 1400 °C and 2100 °C. Depending on the filament material and

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temperature, silane can be completely dissociated into atomic Si and H at the catalyst surface. The created species react further with unreacted SiH_4 in the gas phase, so that various growth precursors are formed. As no ions are generated during deposition, the gas phase species and reactions that occur are different from those in conventional PECVD processes. Furthermore, the absence of any plasma ensures that no particles are trapped, thus eliminating one important source of dust.

Fig. 1 gives a schematic view of a Hot Wire CVD reactor. Summarizing, the most important advantages are:

- The deposition of thin films is plasma-free (i.e. without the risk of a damaging bombardment of energetic ions on the deposited films or of losing functionality of precursor molecules).
- It is an easily scalable method. Scaling to large areas merely requires an increase in catalytic surface along with a proportionally larger supply of source gases.
- Substrates (whether rigid or flexible) can easily be handled as they do not have a role in the decomposition process. Step coverage is excellent, and uniformity can easily be optimized as substrates can be moved during deposition without any difficulty.

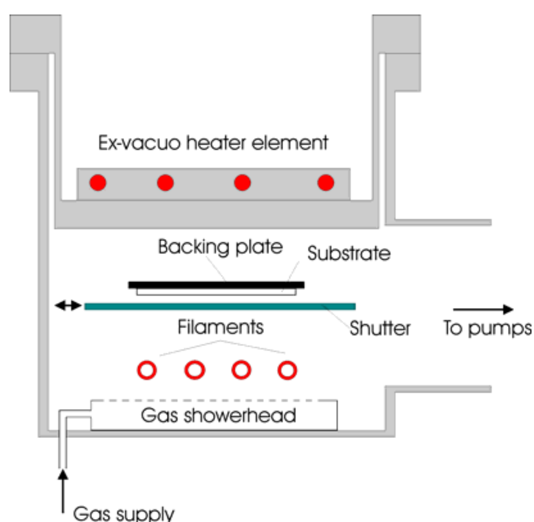

Figure 1. Schematic view of a laboratory Hot Wire Chemical Vapor Reactor.

Ultra high deposition rates of well over 10 nm/s have been obtained in the case of a-Si:H [8]. Additionally, it is possible to deposit amorphous silicon films with a low hydrogen content below 1 at.% that have a low defect density [3]. Solar cells incorporating such layers show less degradation upon light soaking than cells with a conventional PECVD deposited layer [9-11]. These highlights have initiated considerable interest in the HWCVD deposition method and today many groups study HWCVD thin film silicon and its alloys for various applications such as solar cells [12], passivation layers [13], and thin-film transistors [14,15]. A number of applications, such as diamond deposition, functional polymer deposition, and passivating silicon nitride deposition, have already found their way to commercial manufacturing.

A drawback of the HWCVD method in comparison to PECVD is the control of the substrate temperature. Due to the heat radiation from the filaments, it is difficult to use substrate temperatures below 200 °C. Artificial substrate cooling is a possibility, but the

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effects on material quality have not been fully investigated. Another aspect is that reactions of the source gasses with the filaments result in the formation of metal silicides on the filaments. These silicides change the catalytic properties and cause aging of the filaments. Eventually the filaments become brittle, particularly at the relatively "cold" ends of the filament. Any early breakage of the filaments can be prevented by physically shielding the filament ends or by flushing them with hydrogen. Progress has been made in establishing stable and reproducible conditions for the hot catalytic wires used for efficient decomposition of the source gases [16]. By choosing appropriate designs for both the deposition chamber geometry as well as the catalyst geometry, and by an appropriate (pre-)treatment of the filaments, filament lifetime issues can be overcome [17-19].

In this paper, we give examples of progress in HWCVD in three application fields: thin film silicon solar cells, silicon nitride for passivation, encapsulation and isolation, and thin film transistors (TFTs) for active matrix addressing.

Thin Film Silicon Solar Cells

The last few years, we have developed HWCVD intrinsic protocrystalline silicon (proto-Si:H), which is characterized by an enhanced medium range structural order and a higher stability against light-soaking [20] compared to amorphous silicon. We also developed HWCVD nanocrystalline silicon (nc-Si:H), which is characterized by a low density of states [21] at a crystalline volume fraction of ~40% as determined by Raman spectroscopy. These materials were first successfully applied in thin film solar cells on plain stainless steel [19,22].

For single junction 2-μm thick nc-Si:H n-i-p cells we improved the short circuit current density from a value of 15.2 mA/cm^2 for plain stainless steel to 23.4 mA/cm^2 for stainless steel coated with a textured Ag/ZnO back reflector. Secondly, we optimized the nc-Si:H n-type doped layer on this rough back reflector, the n/i interface, and in addition we used a profiling scheme for the H_2/SiH_4 ratio during i-layer deposition. The H_2 dilution during growth was stepwise increased (also called reverse profiling) in order to prevent a transition to amorphous growth. The efficiency that was reached for a single junction nc-Si:H n-i-p cell was 8.6%, which is the highest reported value for hot-wire deposited cells of this kind, whereas the deposition rate of 2.1 Å/s is about twice as high as in record cells with HWCVD nc-Si:H so far. Moreover, these cells are shown to be totally stable under light-soaking conditions.

To enhance the efficiency of solar cells, the use of multibandgap structures is a well proven method in PECVD [23]. Combining the HWCVD technique, a triple junction cell has been obtained with an initial efficiency of 10.9%, see Fig. 2. This cell is a proto-Si/proto-SiGe/nc-Si:H triple junction n-i-p solar cells in which the top and bottom cell i-layers are deposited by Hot-Wire CVD. A schematic picture of the triple junction cell structure is shown in Fig. 3. The cell was deliberately kept very thin (total silicon thickness 2.5 μm). Light-soaking tests show that these triple cells have a light-induced degradation of less than 3.5% [24]. The design is guided by the principle that the non-nanocrystalline cells have to be stable, and therefore these cells have to comprise absorber layers that are protocrystalline (more resistant against light-induced defect formation [25]) and thin (~150-200 nm). This then determines the thickness of the other absorber layers.

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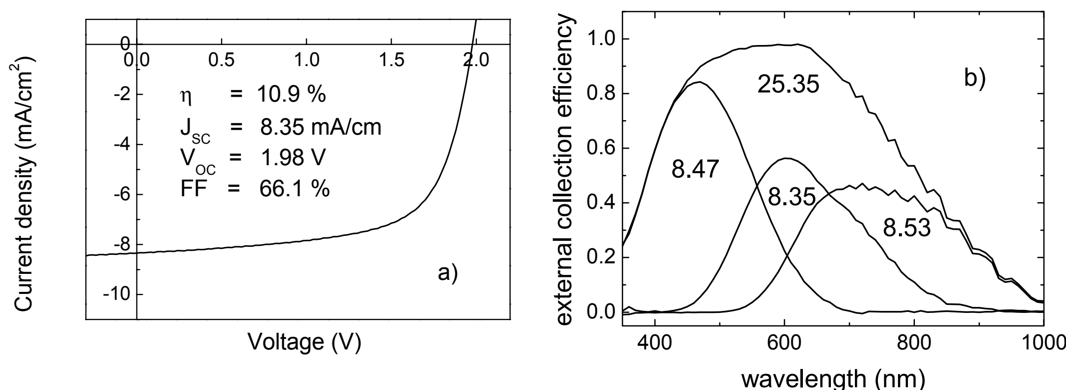

Figure 2: *J-V* (a) and External Collection Efficiency (ECE) (b) of the best triple cell with hot-wire deposited silicon active layers. The values shown in the ECE graph (b) are in mA/cm^2.

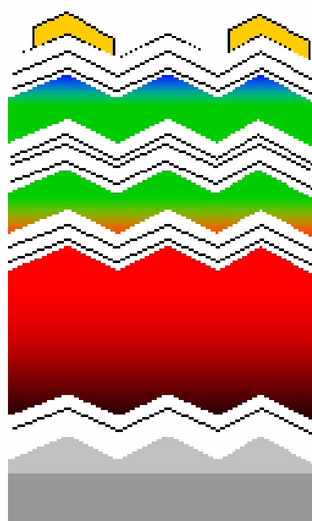

Fig. 3. Schematic cross section of a triple junction thin film solar cell deposited onto a stainless steel substrate with a textured back reflector. The different subcell absorber materials are nc-Si:H, proto-SiGe, and proto-Si (from bottom to top). On top of the silicon layers an indium tinoxide/gold contact is deposited.

Preparation of the Layers and Cells

The silicon layers of the n-i-p structured solar cells were deposited in the PASTA multi-chamber ultra-high vacuum system. Details of the cell structures can be found in previous publications [23,26,27]. Doped layers and intrinsic proto-SiGe:H [27,28] were prepared using 13.56 MHz PECVD, whereas HWCVD was applied to fabricate intrinsic proto-Si:H [22] and nc-Si:H [24,29]. For Hot-Wire deposition, two straight Ta filaments with a diameter of 0.5 mm were used, through which a current of 10.5 A was passed, yielding a wire temperature of 1850 ºC (calibrated in vacuum). The calibrated substrate temperature was 250 ºC. Proto-Si:H was deposited from *undiluted* SiH_4, whereas H_2-diluted SiH_4 was used for nc-Si:H deposition (H_2 dilution (H_2-flow/total gas flow) of around 0.95). The respective deposition rates were 10 Å/s and 2.1 Å/s. The nc-Si:H is a so-called mixed phase or transition material, consisting of nanocrystallites in an a-Si:H matrix [22]. The proto-SiGe:H was first optimized on textured Asahi U-type SnO_2:F substrates conformally coated with Ag and ZnO to provide a constant-quality textured back contact. The source gases for proto-SiGe:H were SiH_4, GeH_4, and H_2. Typical band-gap values of a-SiGe:H are 1.5-1.6 eV [29]. The $GeH_4/(SiH_4+GeH_4)$ flow ratio was 0.45 and the $H_2/(SiH_4+GeH_4)$ ratio was 45. We used an *exponential grading* profile for the GeH_4 flow,

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based on the work described in [30]. Two types of substrates were used: a Ag/ZnO TBR made on stainless steel (SS) foil in our laboratory [31,32] using our in-house Ag/ZnO magnetron sputtering tool SALSA, where the texture of the Ag surface is obtained using elevated substrate temperatures, and a SS/Ag/ZnO substrate provided by United Solar Ovonic LLC Corporation, for comparison.

Indium-tin-oxide served as an anti-reflecting TCO top window; an evaporated gold grid on top served to reduce the sheet resistance. Both the metal oxide layers and the textured Ag of the TBR were deposited by rf magnetron sputtering in our SALSA system [31,32].

Results on Solar Cells

In table I, the parameters of this triple junction cell are compared with a nc-Si:H single junction bottom cell and with a similar triple cell with a nc-Si:H middle cell.

TABLE I. Performance of a n-i-p HWCVD nc-Si:H single junction cell, and triple n-i-p/n-i-p/n-i-p HWCVD proto-Si/proto-SiGe/ HWCVD nc-Si:H and HWCVD proto-Si/HWCVD nc-Si:H/ HWCVD nc-Si:H solar cells on textured Ag/ZnO made in house.

Type of Cell	V_{oc} (V)	FF	J_{sc} (mA/cm^2)	Efficiency (%)
Single junction nc-Si:H n-i-p	0.55	0.67	23.6	8.6
Triple junction proto-Si/ proto-SiGe:H/ nc-Si:H	1.98	0.66	8.35	10.9
Triple junction proto-Si/ nc-Si:H/ nc-Si:H	1.89	0.62	8.15	9.6

Higher initial efficiency can of course be obtained by using thicker active layers for all three cells. However, this is at the risk of reduced stability of the performance. In addition, there is an additional economical advantage for thin cells since the deposition time can be kept shorter. One of the improvements is expected to come from optimization of the middle cell (which is still made with PECVD). At present the middle cell is a limiting factor for the triple cell performance [27].

High Deposition Rate Silicon Nitride

Thin film silicon nitride is a Hot-Wire deposited material that is likely the first to be commercially applied. Many applications are possible for SiN_x. This material has been demonstrated as encapsulation barrier against H_2O and O_2 (even on top of sensitive organic layers) [33], as passivating dielectric in AlGaN/GaN high mobility field effect transistors [34], as a mechanically strong material for microelectromechanical structures (MEMS) [35], as the gate dielectric in thin film transistors (TFTs) [15], and as a passivating antireflective layer on polycrystalline solar cells [13,42]. This section shows the recent progress on the application of SiN_x:H and a-Si:H deposited at high Hot-Wire deposition rates for deposited thin film transistors (TFTs).

Results on Silicon Nitride

The first requirement for obtaining high deposition rate is to obtain a high dissociation rate of the source gasses. Fundamentally, in PECVD, high electron energy is required to fragment molecules while the probability of occurrence is low, since point collisions are required in a 3D space. Hot Wire CVD is fundamentally different since

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molecules are cracked on a 2D catalyst material, which makes it far more probable for each source gas molecule to be decomposed.

The decomposition probability for SiH_4 in a single collision with the filament is 40% [36]. As the number of collisions at commonly used pressures (0.01 mbar) on a catalytic surface of typically 50 cm^2 is close to 10, the overall decomposition probability of SiH_4 molecules in a stagnant gas is close to unity. In practice, taking into account that also the reaction products can be pumped out, the total gas utilization efficiency for a-Si:H deposition from SiH_4 can be as high as ~80%, as is observed experimentally [37]. This utilization rate is ~5 times larger than in PECVD.

For a SiH_4/NH_3 mixture at relatively low total flow rate, and thus low deposition rate, utilization rates of 98% and 52% for SiH_4 and NH_3 have been obtained, respectively [38]. At a high deposition rate (3.0 nm/s) we still have a SiH_4 utilization rate of > 70% [39]. Good gas utilization and high deposition rate are highly desirable from a cost point of view. The efficient catalytic decomposition of feedstock gasses has led to ultrahigh deposition rates of up to 7.3 nm/s for device quality, transparent, near-stoichiometric films [40]. The application of HW-SiN_x at a deposition rate of 3 nm/s to polycrystalline Si wafer solar cells has led to cells with 15.7% efficiency in collaboration with the Energy research Center of the Netherlands (ECN) [41]. The 7.3 nm/s material has also been tested as passivating layer on polycrystalline silicon cells in collaboration with Centrotherm Photovoltaics Technology GmbH, Germany, leading to poly-Si cells with 14.9% efficiency [42].

The low H concentration of 9 at.-%, specifically the low density of Si-H bonds [43], is an advantage for the use as sidewall and liner material in ultra large scale integration p-type metal-oxide-semiconductor transistors. This is the case because H, coming from the SiN_x at the sidewalls, can create defects at the gate/gate-insulator interface [44].

Mechanical Stress and rms roughness in HW-SiN_x

For our HWCVD SiN_x films the intrinsic stress is *tensile* for SiN_x depositions with $1.2 < x < 1.6$. We assume that the thermal stress in a SiN_x film does not depend on composition in this range and amounts to -240 MPa (compressive) for films deposited at a substrate temperature of 450ºC. A linear dependence of the stress with increasing x is found, with the largest stress for the most N-rich samples. For layers with N/Si = 1.2 the tensile stress becomes as low as 16 MPa. Mechanical stress is an important issue. SiN_x films deposited with conventional methods like PECVD tend to have high stress values in the range of 100–1000 MPa [45]. Passivating layers for organic light emitting diodes for example, require very low stress in the order of 10 MPa [46,47], in addition to low deposition temperatures. Low stress in thin films is also important in micro-electro-mechanical (MEMS) applications, plastic electronics and when TFTs are deposited on thin polymer foil.

The root-mean-square (rms) roughness (as determined by atomic force microscopy (AFM)) measured on 300 nm thick $SiN_{1.3}$ layers is about 1 nm. A low rms value is necessary for high field-effect mobility in thin film transistors, for more N-rich layers (x >1.4) lower *rms* values of 0.5 nm are found.

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Thin Film Transistors by Hot Wire CVD

It has been reported earlier that TFTs with thermally grown SiO_2 on c-Si as gate dielectric with HWCVD a-Si as conducting channel, are electronically more stable than when the a-Si is made with PECVD [14,48]. The thin-film alternative for the thermally oxidized wafer is SiN_x on glass, made with HWCVD, because then both the dielectric film and the a-Si conducting channel can be made with HWCVD. The application of this very fast and easy scalable technique for all layers decreases processing time greatly. A disadvantage of PECVD is that it may lead to SiN_x materials that are too porous as well as too H-rich at high N concentration [49].

TFTs exclusively made with HWCVD have been investigated in the past and showed good performance and stability [50,51]. Here, we report on results of “all hot wire TFTs“ with amorphous hydrogenated SiN_x as the gate dielectric, made at very fast rates of up to 3 nm/s and a-Si:H as conductive channel made at a very fast rate of 1 nm/s.

Nishizaki *et al.* [15] showed that a-Si TFTs made with HWCVD, show high stability upon bias stressing and that the threshold voltage shift is due to charge trapping in the SiN_x only. To quantify trapped charges and to optimize our HWCVD SiN_x deposited at high deposition rates (~3 nm/s), we determined the mechanical stress, the root-mean-square (*rms*) roughness and the dielectric properties including fixed and trapped charges of our HWCVD SiN_x for various compositions.

Thin SiN_x films deposited using HWCVD have a maximum in mass density and a minimum in H concentration at an atomic N/Si ratio of 1.3 [40]. For this reason we selected this material for testing in TFTs. Trilayer TFT structures in bottom gate staggered configuration have been made, the structure is shown in Figure 4. The structure consists of HWCVD $SiN_{1.3}$ (made at 3 nm/s), HWCVD a-Si:H (made at 1 nm/s) [52] and PECVD μc-Si:H highly doped n-layers. For the HWCVD SiN_x/a-Si:H stack this leads to a total deposition time of less than 4 minutes. The depositions were performed at Utrecht Solar Energy Laboratory (USEL) on Corning 1737 glass with pre-patterned 100 nm thick Cr gates as provided by Japan Institute of Advanced Science and Technology (JAIST). After deposition of the HWCVD films, the photolithographic structuring was performed at JAIST. Unfortunately, it was necessary to introduce an air break between the SiN_x deposition and the a-Si:H deposition, which most likely posed an upper limit to the achievable mobility. In these first experiments, the SiN_x gate insulation was made thick (400 nm), to avoid electrical breakdown of SiN_x. The result is that no pinholes have been found within the matrix made (86 TFTs) but the S-value is rather large (1 V/decade). Analysis shows that these “all hot wire” TFTs have an on/off ratio of 10^6 and a mobility of 0.4 cm^2/Vs after a forming gas anneal, the transfer characteristics of the TFTs were measured three times.

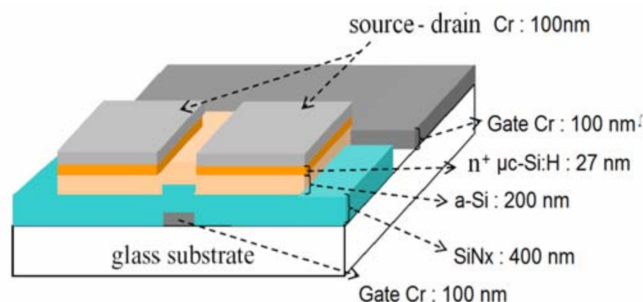

Figure 4. Schematic diagram of the trilayer structure made by USEL and JAIST.

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The transfer characteristics are shown in Figure 5. The subsequent curves correspond to the first, second, and third measurement. The threshold voltage is slightly increased in the direction of more positive gate voltage after each measurement.

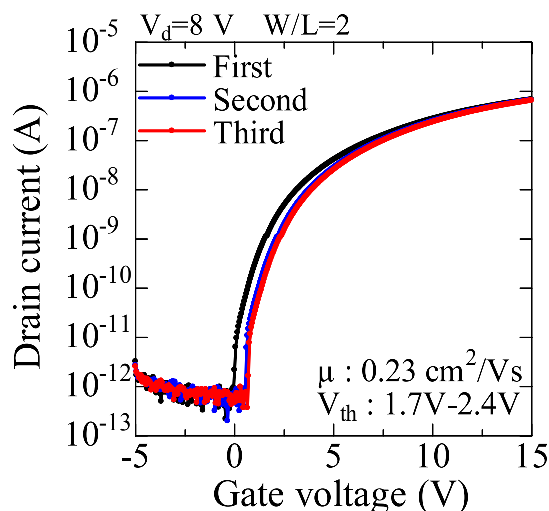

Figure 5. Transfer characteristics of the HWCVD SiN_x/a-Si:H TFT, before forming gas anneal.

It is known that the V_{th} shift caused by charge trapping is dependent on the composition of the SiN_x dielectric in the case of plasma-deposited films [53] and a study of the defect density and bond structure specifically for hot-wire deposited SiN_x was done at JAIST [15]. It is shown that V_{th} shift can be minimized by carefully optimizing the composition of the SiN_x. The present TFT data are consistent with a composition of the SiN_x film that is neither too Si rich nor too N rich, since the initial V_{th} shift is very small.

The S-value is rather large, but this is due to the large thickness (400 nm) of the SiN_x film. The series resistance of the source and drain contacts is very low because of the use of microcrystalline n-type source and drain contact layers. The mobility (in Table 1) is estimated from the gradient of the square root of I_d as a function of V_g in the saturation region (V_d = 8 V).

We annealed the TFTs in forming gas (H_2/N_2) at 200°C for two hours. Afterwards, the mobility was measured in three different ways. The first method uses the I_d –V_d data in the linear regime. The second method uses the transconductance g_m, at constant V_g, The third method is based on the output characteristics around V_d = 0. This method could be used because the contacts had very low Ohmic resistance. Table I shows the mobilities obtained by all three methods, before and after forming gas anneal. The three methods show consistent results and it is seen that the highest measured mobility is 0.4 cm^2/Vs.

These TFTs show that HWCVD SiN_x, deposited at 3 nm/s is already suitable for application in TFTs. To determine whether x = 1.3 (as used in the TFTs described above) is the optimal N/Si ratio, stress, *rms* roughness and electrical measurements are performed.

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TABLE II. Mobility (cm^2/Vs) determined by three different methods, both before and after forming gas anneal.

Mobility determination:	**Method 1**		**Method 2**		**Method 3**	
Anneal:	**Before**	**After**	**Before**	**After**	**Before**	**After**
W/L = 2	0.29	0.34	0.32	0.38	0.31	0.34
W/L = 50	0.17	0.29	0.18	0.32	0.18	0.31

In line Hot Wire CVD

We have conducted preliminary investigations on the feasibility of performing a HWCVD process uniformly on *moving* Corning 2000 glass (for optoelectrical characterization and displays) or TCO-coated glass substrates (for solar cell fabrication). As the creation of charged dust particles in the gas phase is avoided in HWCVD, deposition could be undertaken with the substrates facing *upward* (this is at variance with Figure 1), thus further simplifying the mounting of the substrates. The deposition experiments have been conducted in our PILOT system, a two-chamber plus load lock system, originally installed to produce homogeneous thin film silicon layers on a 30 cm x 40 cm substrate PECVD. The transport system utilizes rails to guide the substrate holder between chambers or within one of the chambers. The holder can be pushed or pulled along the rail system by a transport arm, thus allowing the movement of substrates *during* deposition, by which in-line manufacturing can be mimicked. The "intrinsic" chamber (or i-chamber) was adapted to accommodate a hot-wire assembly while keeping the original rf electrode in place. For the purpose of hot-wire deposition, multiple, parallel, 99.9 % pure Ta filaments with a diameter of 0.50 mm were mounted above the substrate transport system.

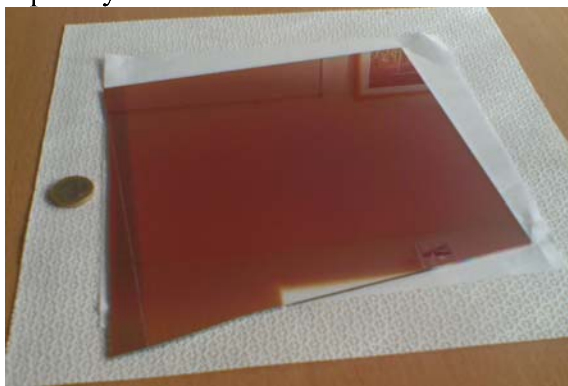

Figure 6. An a-Si:H thin film with device-quality properties made on moving glass substrate (~20 cm x ~20 cm; a one Euro coin is added for reference).

Above the filament assembly, a shower head gas supply is mounted to achieve an evenly distributed feedstock gas flow.

Fig. 6 shows an amorphous silicon thin film deposited on a plain glass substrate while it was moving under the filaments. The dark and photoconductivity of amorphous silicon on moving glass substrates were $\sigma_d = 8 \bullet 10^{-12}\ \Omega^{-1}cm^{-1}$ and $\sigma_{ph} = 1.9 \bullet 10^{-6}\ \Omega^{-1}cm^{-1}$ (showing an appropriate photoresponse for solar cell applications, in excess of 10^5) and

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the dark activation energy was E_a = 0.92 eV, which indicates the intrinsic property of this material, having a band gap of 1.85 eV [54]. Microcrystalline silicon on moving glass substrates had dark and photoconductivities, respectively, of $\sigma_d = 2.2 \bullet 10^{-7}\ \Omega^{-1}cm^{-1}$ and $\sigma_{ph} = 4.0 \bullet 10^{-5}\ \Omega^{-1}cm^{-1}$ (photoresponse of ~200). The dark activation energy was E_a = 0.6 eV, again indicating a Fermi level position close to mid gap. The Raman crystalline fraction was 0.68.

To test these films, we ventured the demonstration of p-i-n solar cells. We used standard Asahi U-type TCO-coated glass substrates. The p- and n-layer were made by (stationary) PECVD in another chamber of this system. For the intrinsic layers we used the processing conditions for amorphous silicon on moving substrates. Despite the two air breaks that were needed because the PECVD is performed with the substrates facing down while the HWCVD is done with the substrate facing up, the solar cells performed very well already with our first attempt.

The efficiency was 7.1%, the short circuit current density (J_{sc}) was 15.0 mA/cm^2, the open circuit voltage (V_{oc}) was 0.71 V, and the fill factor was 0.67. The thickness of the i-layer was ~300 nm. While the V_{oc} is rather low, which is attributed to the need to have air breaks at the p/i and i/n interfaces, the fill factor is not influenced by the two air breaks.

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