EUROPEAN RECORD EFFICIENCY AMORPHOUS-CRYSTALLINE-SILICON HETEROJUNCTION SOLAR CELLS: FINAL RESULTS FROM THE HETSI PROJECT

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In this work, we present some of the main results obtained within the project "*Heterojunction Solar Cells based on a-Si/c-Si*" (HETSI) [1], funded by the European Commission in the framework of the 7th Research Framework Program from 2008 to 2011. This project, based on the promising silicon heterojunction technology, represents a concerted effort of the consortium, a well balanced mix of universities, institutes of technology and industrial partners, to combine device modelling, material optimization and characterization, process development (from texturization to metallization), PV cell and module process integration, while cost and environmental issues are addressed as well.

Thanks to a better understanding of the device physics from advanced characterization tools and modeling, the results obtained by this consortium have put Europe on the map, with a record cell efficiency of 20,7% on large area n-type c-Si wafers. Moreover, a dedicated module process has been developed with low losses of only 1% absolute from cell to module.

Keywords: Heterojunction, solar cell, silicon

1 INTRODUCTION

Amorphous/crystalline (a-Si:H/c-Si) silicon heterojunction solar cells (HET) are attracting more and more attention due to the combination of several advantages: low temperature process suitable with reduction of wafer thicknesses (cost reduction), compatibility with industrial requirements (high throughput, large solar cells area), excellent surface passivation, simple process-flow (no selective openings needed) and very high efficiencies. Efficiencies up to 25% can be achieved by the silicon heterojunction solar cell concept [2] and Sanyo has demonstrated recently 23% in laboratory using the so-called HIT[tm] structure on n-type c-Si [3].

The key feature of this structure is the insertion of a thin intrinsic a-Si:H layer between the c-Si substrate and the a-Si:H(p) emitter to reduce the density of defects at the hetero-interface of the device. This allows obtaining open-circuit voltage values as high as 730mV [4]. Many research groups are currently working on a-Si:H/c-Si heterojunction solar cells either on p or n-type substrate [5-9] with a considerable improvement of the solar cell efficiency obtained in recent years.

One such consortium has received funding from the European Commission in the framework of the 7th Research Framework Programme to develop a knowledge base and optimized device structure based on new insights in the physics and technology of wafer-based silicon heterojunction devices, within the project "*Heterojunction Solar Cells based on a-Si c-Si*" (HETSI) [1].

This paper describes the major achievements on all aspects of heterojunction a-Si/c-Si cells obtained during the project by the consortium. Details of obtained results and a thorough description of the state-of-the-art in amorphous-crystalline heterostructure silicon solar cells can be found in [25], and papers referenced herein.

2 EXPERIMENTAL and RESULTS

2.1 Characterization and modeling
2.1.1 CP-AFM characterization

In order to investigate the electronic properties of the a-Si:H/c-Si heterointerface, conductive probe atomic force microscopy (CP-AFM) was used on symmetrical ITO/a-Si:H/c-Si/a-Si:H/ITO samples. These consisted of (p) a-Si:H/(n) c-Si/ (p) a-Si:H stacks with a-Si:H thicknesses ranging from 20 to 300 nm. The samples were cleaved, and the AFM tip was swept over the cleaved section across the interfaces, as indicated in Figure 1.

Figure 2 shows an example of recorded images at the (n) a-Si:H/(p) c-Si interface. A conductive channel is clearly observed in the c-Si at the interface. It originates from a strong inversion region at the c-Si surface due to the strong band bending at the heterojunction.

Using 1D modelling through AFORS-HET [10] and analytical calculations, the band bending and the free carrier densities could be computed in the (p) a-Si:H/ (n) c-Si structure as a function of the valence band offset. One can observe that strong inversion requires the valence band offset, ΔE_V, to be large enough (>0.25 eV). This lower limit value is in agreement with the determination ($\Delta E_V = 0.4$ eV) deduced from the analysis of the temperature dependence of planar conductance measurements.[11-13] and $\Delta E_V = 0.46$ eV as measured with near-UV photoelectron spectroscopy [14,15].
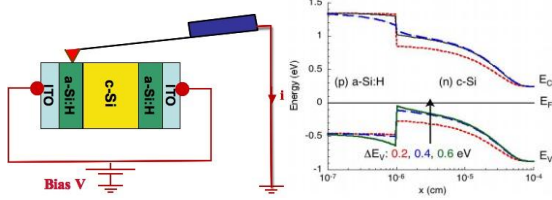

Figure 1: The CP-AFM technique was used to sweep the tip across the a-Si:H/c-Si interface on cleaved sample sections (left). The band bending at the (p) a-Si:H/ (n) c-Si interface is strongly dependent on the valence band offset (right).
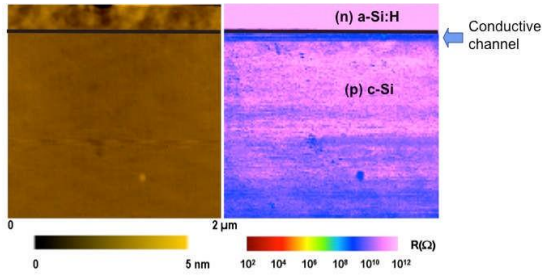

Figure 2: Topography (left) and local resistance (right) mapping of the (n) a-Si:H/(p) c-Si interface

2.1.2 QSSPC characterization and modeling

QSSPC (Quasi Steady State Photoconductance Decay), is a well known characterization technique in the field [16]. A round-robin was conducted, i.e. a campaign of measurements based on samples produced by several partners of the project and analysed by the same kind of set-up, namely the Sinton WCT, at each partner's lab. The results proved that the charge carrier vs. excess carrier density data can be measured very reliably with the set-up, deviations between the set-ups at the different labs were small. The set-up can thus be used as a standard characterization tool for the passivation properties of a-Si:H/c-Si interfaces. In parallel, a model was developed to help analyzing the data issued from these measurements [17]. It allows one to quickly extract both the interface state densities that govern defect-induced recombination of carriers and the effective charge (located in the a-Si:H layer and in the interface states) that determines the band bending and the so-called field effect passivation. Applying this model to experimental data obtained on a set of symmetric *a*-Si:H(p)/*a*-Si:H(i)/*c*-Si(n) stacks, as used in high efficiency solar cells (figure 3), it was possible to identify the predominant passivation mechanism of these stacks depending on the i-layer thickness and on the emitter doping [18]. Thus, it was concluded that, in the absence of (i) a-Si:H interlayer the interface defect density increases with doping of the a-Si:H layer, explaining the

decrease in effective lifetime at an excess carrier density of 10^{15} cm^{-3} observed in Figure 3, while the negative impact of the doping can be shielded by the (i) layer. With a 10 nm thick i-layer, the interface is well passivated for all doping densities, and the increase in lifetime can be attributed solely to field-effect passivation.
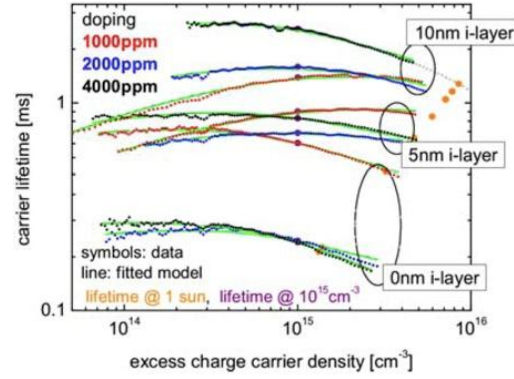

Figure 3: Lifetime data for samples with varying i-layer thickness and emitter doping (symbols) and simulated lifetime curves (lines). Highlighted are the lifetime values at 10^{15} cm^{-3} and at one sun.

2.2 Transparent conductive oxides

The main role of the Transparent Conducting Oxides (TCOs) on a-Si:H/c-Si heterojunction (HJ) solar cells is to provide sufficient lateral electrical conductivity towards the grid fingers, combined with high optical transparency and low reflection losses to enhance photon absorption. These two properties are mutually exclusive, and few are the materials that can combine such features. The TCO must also have a work function adapted both to the charge carrier's electronic level in the semiconductor (a-Si:H), and to the metal work function to provide optimized carrier collection. During the project, Indium Tin Oxide (ITO), Aluminum Zinc Oxide (AZO) deposited by PVD and Boron Zinc Oxide (BZO) deposited by MOCVD, have been evaluated [19]. ITO has been identified to be the best candidate, especially for the front side. A good compromise of the electrical and optical properties for the front TCO (even if also metallisation has to be taken into account) to reach 21% efficiency on a-Si:H/c-Si heterojunction solar cells is shown in table 1:

n (633)	k (633)	n (1000)	k (1000)	μ cm²/Vs	N x20cm^{-3}	ρ $\Omega \cdot$cm	Φ eV
>1.98	<0.05	>1.85	<0.05	>30	<2	<5e-4	>4.8

Table 1 : Properties of the front TCO to ensure good J_{sc} and FF values for Si HET solar cells, in order to reach 21% efficiency : real and imaginary parts (n and k) of the optical index at 633 and 1000 nm, electron mobility (μ) and density (N), resistivity (ρ) and work function (Φ).

We also investigated the structural properties of the different types of TCO layers by means of XRD measurements.
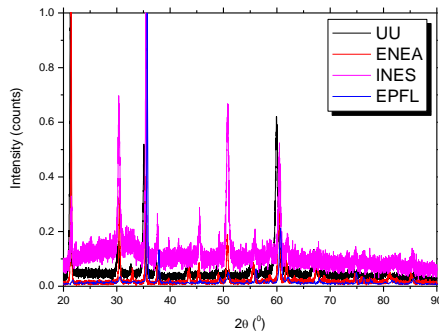
Figure 4 : Normalized XRD patterns of ITO layers.

For the ITO layers, a strongly varying composition has been observed, with various diffraction peaks, indicating the presence of the associated crystal planes in the material, emerging for the different samples (see Figure 4). From the data, it could be observed that the layers with a relatively strong (211) peak (made by UU and ENEA) showed a higher electron mobility than the layers with a relatively strong (400) peak (INES and EPFL). These variations could be attributed to the different process parameters and oxygen partial pressure during PVD deposition.

2.3 Surface conditioning, and passivation

As already described, an efficient cleaning of the surface is mandatory to obtain high passivation level by the deposition of an amorphous silicon layer. Indeed, the c-Si surface density of states should be as low as possible, and this is directly correlated to an efficient cleaning prior to the hydrogen rich amorphous silicon layers.

CEA-INES developed a simplified and optimised wet-chemistry cleaning recipe for industrial applications. Using such a cleaning improved the extrapolated open circuit voltage (V_{oc}) values from 730 mV to > 740-745 mV. A gain of 10 mV was confirmed by direct measurements on solar cells. [20].

The passivation properties of a-Si:H layers are also a key point to obtain high efficiency solar cells(cf. Fig. 3).

EPFL found that passivation follows stretched-exponential dynamics upon hot plate annealing. From this, it was inferred that the surface passivation occurs by hydrogenation of c-Si surface states [21]. Doping amorphous silicon layers often leads to inferior passivation, however [22].

Next, EPFL has been able to establish a link between plasma properties and film quality [23]. It was observed that highly depleted plasmas lead to the best passivation, and that the silane depletion of the plasma is a more fundamental parameter than the power or pressure of gas flows.

As such, excellent passivation levels have been obtained in both RF and VHF PECVD reactors, as evidenced by carrier lifetime values well above 5 ms, corresponding to implied V_{oc}s > 730mV.

2.4 Large area cell process integration

To produce solar cells, high quality FZ and CZ n-type monocrystalline wafers have been used (<100>; 200 μm; 1-5 Ohm·cm).

The wafers were first randomly textured by a classical KOH-IPA wet process. Prior to the a-Si:H deposition, a multistep cleaning (RCA+) was applied just before processing the front and back side, followed by an HF dip to remove the native oxide and saturate surface dangling bonds by hydrogen.

The (n) and (p) a-Si:H layers were deposited at 200°C from $SiH_4/H_2/PH_3$ and $SiH_4/H_2/B_2H_6$ doping gas mixtures, respectively. A thin buffer layer was deposited on both sides, prior to the doped layers. An 80 nm thick ITO layer (ITO) deposited by DC magnetron sputtering was used at the front side while ZnO(B) was applied at the back side of the solar cells. Finally, 500nm of sputtered Al on the whole surface forms the back contact of the cell and an Ag-paste is deposited by screen printing through an optimized designed grid on the front side.

At EPFL 2x2 cm^2 cells on 8x8 cm2 wafers with efficiencies >20% were obtained in an industrially-sized 40x50 cm^2 VHF reactor with ITO on both sides. V_{oc} values up to 717 mV have been obtained. At INES, a solar cell process was developed that is scalable to very large area reactors (up to 2*2 m^2). On 100.5 cm^2 FZ wafers, this has resulted in efficiencies as high as 20,7% (Figure 7) with screen printed lines at the front of the solar cell. Up to 732 mV V_{oc} values have been obtained, which to our knowledge is the second world best performance ever obtained behind Sanyo's record value.
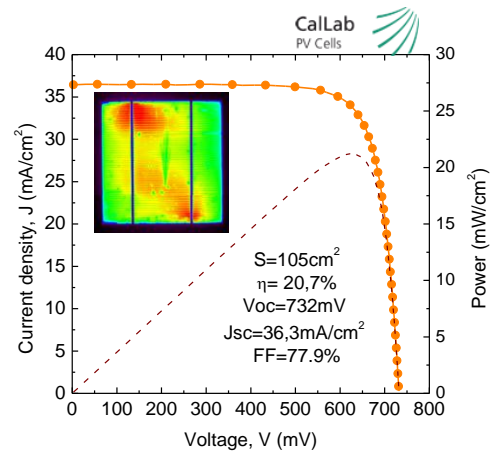

Figure 7: I(V) curve of the best solar cell with record V_{oc} up to 732 mV. The insert shows an Electroluminescence picture of the corresponding solar cell.

2.5 Module technology

To produce modules from hetero junction cells, innovative interconnection and encapsulation processes must be developed. The metallization of heterojunction solar cells is done with low-temperature silver polymer screen printed pastes. The classical soldering steps to interconnect the cells will be problematic since these pastes cannot be soldered: soldering temperatures would destroy the solar cell. Conductive adhesive curing at low temperatures is a very promising candidate for the interconnection of thin and temperature sensitive solar cells such as silicon HET cells. In order to validate this choice, TLM tests were conducted to evaluate the contact resistance (Tab. 2). From this experiment, we can conclude that contact resistance is sufficiently low to be applied in PV modules.

adhesive	curing profile	R_c measured $(m\Omega)$	specific R_c $[\Omega cm^2]$
Acrylic A	oven: 10 min @ 130°C	1.57	9.0×10^{-5}
Epoxy B	oven: 10 min @ 130°C	1.40	8.1×10^{-5}
Epoxy C	45 min @ 130°C	0.91	5.2×10^{-5}

Table 2 : Summary of selected adhesives.

Concerning encapsulation, it is well known that Transparent Conductive Oxides can be sensitive to moisture ingress. In order to demonstrate long term stability of the modules, special care was taken by designing a novel module in order to prevent moisture ingress through the back sheet foil. A thin foil of aluminium was integrated in the module back sheet. The **'novel A'** module design for hetero junction cells consists of (from top to bottom) a 4 mm top glass plate, 400 μm EVA, HET cells and interconnection, 400 μm EVA, PET layer, Aluminium and finally a PVF (Tedlar) back-sheet. Additionally, in **'module B'**, standard technology was applied to build a module from the HET cells, acting as a reference material for the climatic chamber tests. The standard module consists of (from top to bottom) 4 mm top glass plate, 400 μm EVA, hetero-junction cells and interconnection, 400 μm EVA, and a TPT (Tedlar/PET/Tedlar) back-sheet. The standard module described is the most common packaging technique in industry regarding PV solar modules.

The modules have been exposed to climate chamber tests (damp-heat and thermal cycling) according to the IEC 61215 standard. The results showed virtually no degradation as the power loss stays well within the 5% limit as dictated by the IEC 61215 protocol. Selected back-sheet (Novel A) demonstrated that the modules could survive 1500 hours (1.5 times IEC) of damp heat. On the contrary, the standard module (B) was not capable to pass 500 hours of damp heat. [24]

Finally, in the case of a module with a 2x2 configuration (Figure 10), the target of 1% absolute was reached. The Isc of the 2x2 configuration demonstrates that no loss occurs between cell and module. A fill factor loss of 5,44% was calculated and Voc reduced with 0,43% respectively.

Figure 10 : Photograph of ECN manufactured module with INES hetero- junction cells

3.5 Life cycle analysis

In this task the expected environmental impact of the most promising process flow for cells and modules is calculated. Furthermore the energy pay-back time of the silicon heterojunction technology for cells and modules is calculated and compared to standard solar cells on monocrystalline silicon. The relative contributions to the cumulative energy demand of the main cell and module process steps are compared and the global warming potentials are calculated (shown in Figures 8 and 9).
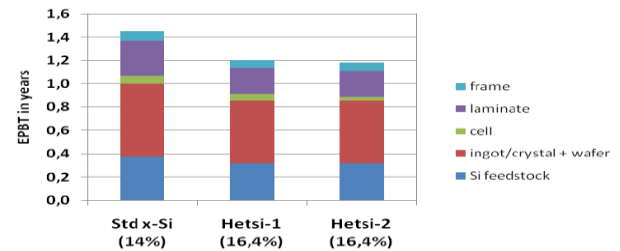

Figure 8: Calculation of the energy pay-back time for standard mono silicon and silicon heterojunction solar cells based on an insolation of 1700kWh/yr.
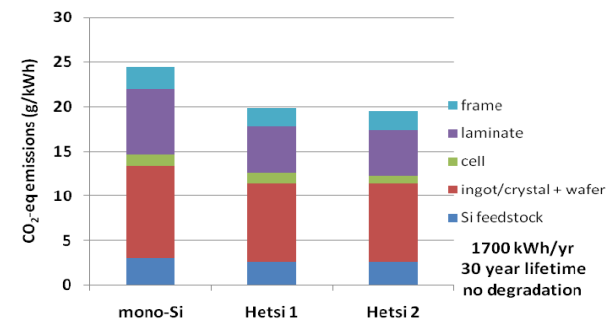

Figure 9: Comparison of CO_2 emission equivalents for mono silicon solar cells and silicon heterojunction module manufacturing (BOS not included).

We conclude that the cumulative energy demand and the global warming potential of the heterojunction technology require similar amounts of energy and produce similar amounts of CO_2-equivalent of global warming gases compared to mono c-Si. The high efficiency of the heterojunction solar cells factors into a more favorable energy payback time, and a lower carbon footprint.

3   CONCLUSIONS

In this work we have presented the main results obtained within the HETSI project on silicon heterojunction solar cells. A better understanding of the device's physics has allowed the consortium to improve the solar cell efficiency up to 20.7% with open circuit voltage values up to 732 mV, and to establish an innovative module process flow.

4   ACKNOWLEDGEMENTS

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