

# 3.4

## Heterojunction Silicon Solar Cells

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Silicon-based solar cells are predominantly of the so-called homojunction type, i.e., the junction is made so that the material on either side of the junction is the same, albeit that doping levels and type can be different, see also Part 2 in this book. When two different semiconductor materials form a junction, where the materials differ in bandgap, it is denoted as a heterojunction, and this results in band offsets and band discontinuities. Heterojunctions were first discussed in the 1950s (Sze, 1981; Kroemer, 2000) and they have found widespread applications in, among others, lasers, light emitting diodes, and solar cells. The latter will be discussed here.

Heterojunctions can be found in a wide variety of solar cells. Examples include the Heterojunction with Intrinsic Thin-layer (HIT) solar cell, which is based on a thin amorphous silicon p-type doped layer on top of an n-type doped c-Si wafer (Van Sark *et al.*, 2012; De Wolf, 2012), the cadmium telluride (CdTe/CdS) and copper indium (Ga) diselenide (CIGS/CdS) solar cell (Scheer and Schock, 2011; see also Part 4) and the bulk heterojunction organic PV (Part 6). Heterojunctions are also encountered in multijunction solar cells (Part 8). High efficiency cells have been demonstrated with >40% efficiency using material alloys from Groups III and V of the Periodic Table (Philipps and Bett, 2014).

The silicon heterojunction cell (SHJ), also commonly termed the HIT cell (a trademark of the Panasonic Company), can best be characterized as a device structure that combines the best of thin film (Part 5) and bulk silicon technology. It has been referred to as a marriage between these two technologies and was first announced as a “honeymoon” cell (Hamakawa *et al.*, 1983; Tanaka *et al.*, 1992). Early patenting has given Sanyo a head start in commercializing the SHJ technology, which is now marketed by Panasonic. When the SHJ technology is combined with a backside contact structure, it has been demonstrated to result in 25.6% efficiency, the highest “one-sun” efficiency to date for a crystalline silicon solar cell (Masuko

*et al.*, 2014). Interestingly, another record efficiency of 25.1% for a two-sided contacted SHJ cell was reported by Kaneka (Yamamoto *et al.*, 2015).

In this chapter, first, the basics of heterojunctions will be presented, drawing on the basics of homojunctions presented in Part 2. The subsequent sections will present the development of the SHJ cell.

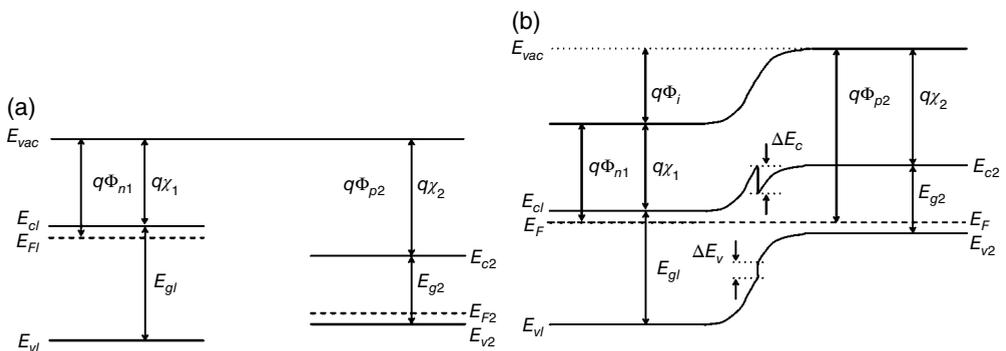
### 3.4.1 Basic Principles

We consider the energy band diagram of a *pn* heterojunction in Figure 3.4.1 (Muller *et al.*, 2003). An isotype heterojunction, where doping type of both materials is the same, i.e., an n+n or p+p junction, is not treated here. Figure 3.4.1 (a) shows the energy band diagram of the two separated semiconductors that will form the *pn* heterojunction, i.e., a wide bandgap *n*-type semiconductor on the left and a narrow bandgap *p*-type semiconductor on the right with bandgaps  $E_{g1}$  and  $E_{g2}$ , respectively, with  $E_{g1} \neq E_{g2}$ . In the general case, the electron affinities of the materials can be different, i.e.,  $\chi_1 \neq \chi_2$ . Doping densities are  $N_{d1}$  and  $N_{a2}$ . Also note that the conduction band edge of the wide bandgap material is higher in energy than that of the narrow bandgap material, and vice versa for the valence band edges.

When the two materials are brought together, electrons and holes will flow, leaving a depletion region at the junction between the materials just as in the homojunction case (Chapter 2.6), and thermal equilibrium is reached, which is clear from the Fermi level  $E_F$  that is the same at both sides of the junction (Figure 3.4.1 (b)). Unlike with the homojunction, this leads to band edge discontinuities of the conduction and valence band at the junction. In the case shown in Figure 3.4.1 (b), we notice what is called a “spike” and a “notch” in the conduction band, in which free charges could accumulate. The magnitude of  $\Delta E_c$  is determined by the doping levels on either side of the junction.

The resulting built-in voltage  $\Phi_i$  (also denoted as  $V_{bi}$ ) can be found as follows:

$$q\Phi_i = q\Phi_{p2} - q\Phi_{n1} = (q\chi_2 + E_{c2} - E_F) - (q\chi_1 + E_{c1} - E_F) \tag{3.4.1}$$



**Figure 3.4.1** Energy band diagrams for a heterojunction. (a) Two separated semiconductors, with a wide bandgap *n*-type semiconductor on the left and a narrow band gap *p*-type semiconductor on the right. (b) Energy levels after bringing the materials into contact and reaching an equilibrium state. The vacuum level remains continuous, while the conduction and valence band are discontinuous. Source: Adapted from Muller *et al.* (2003)

with

$$E_{c1} - E_F = kT \ln \left( \frac{N_{c1}}{N_{d1}} \right) \quad (3.4.2)$$

$$E_{c2} - E_F = E_{g2} - (E_F - E_{v2}) = E_{g2} - kT \ln \left( \frac{N_{v2}}{N_{a2}} \right) \quad (3.4.3)$$

with  $N_{c1}$  and  $N_{v2}$  being the effective density of states at the conduction and valence band edges of the two materials.

Combined with Equations (3.4.2) and (3.4.3), Equation (3.4.1) becomes:

$$\Phi_i = \chi_2 - \chi_1 + \frac{1}{q} \left( E_{g2} - kT \ln \left( \frac{N_{c1} N_{v2}}{N_{d1} N_{a2}} \right) \right) \quad (3.4.4)$$

For the case that the electron affinities of both materials are equal, the discontinuity in the conduction band disappears and Equation (3.4.4) is reduced to a similar form as was derived for a homojunction, except that a term with  $E_{g2}$  remains:

$$\Phi_i = \frac{1}{q} \left( E_{g2} + kT \ln \left( \frac{N_{d1} N_{a2}}{N_{c1} N_{v2}} \right) \right) \quad (3.4.5)$$

where it should be noted that the product  $N_{c1} N_{v2}$  would equal the intrinsic carrier density squared ( $n_i^2$ ) if both materials were the same (the homojunction case, see Chapter 2.6).

The potential drop is divided over the two sides as follows (Muller *et al.*, 2003):

$$\Phi_{i1} = \Phi_i \frac{\varepsilon_2 N_{a2}}{\varepsilon_1 N_{d1} + \varepsilon_2 N_{a2}} \quad (3.4.6)$$

$$\Phi_{i2} = \Phi_i \frac{\varepsilon_1 N_{d1}}{\varepsilon_1 N_{d1} + \varepsilon_2 N_{a2}} \quad (3.4.7)$$

with  $\varepsilon_1$  and  $\varepsilon_2$  the permittivities of the two materials. As with the homojunction, the built-in voltage drop is larger across the material with the lightest doping concentration. This is important in a heterojunction due to the presence of a spike in the conduction band edges. For example, when the doping in material 1 is higher than that in material 2, most of the band bending occurs in material 2, leading to the fact that the top of the spike is lower than the conduction band edge of material 2 (see Figure 3.4.1(b)) (Muller *et al.*, 2003). This influences the operational performance of heterojunction devices, such as solar cells. Proper analysis of band diagrams thus is necessary to understand device performance. The current across the junction can be expressed in a similar way as for homojunctions (Chapter 2.6), albeit that electron and hole currents are dependent on the band discontinuities in the conduction band (Muller *et al.*, 2003).

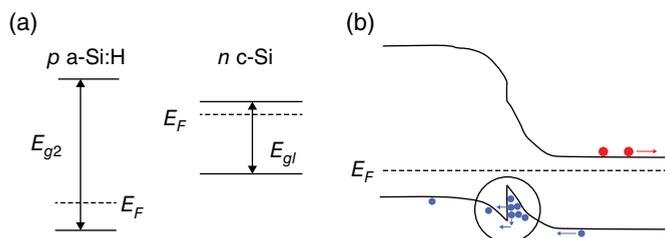
### 3.4.2 a-Si:H/c-Si Cell Development

The silicon heterojunction solar cell is based on a device structure that combines thin film and bulk silicon technology. Of particular interest is the heterojunction cell with an intrinsic thin layer (HIT) (Tanaka *et al.*, 1992) with which Sanyo had achieved a very high efficiency of 23% in 2009 (Taguchi *et al.*, 2009), and of 25.6% efficiency most recently (Masuko *et al.*, 2014). This strongly challenges the standard high efficiency c-Si homojunction cell (Green *et al.*, 2015). The emitter can be an amorphous (Taguchi *et al.*, 2009) or microcrystalline (Van Kleef *et al.*, 1997) silicon type. It is claimed by Sanyo (Tanaka *et al.*, 1992) that an excellent surface passivation of c-Si at the c-Si/a-Si interface is most important for high efficiency.

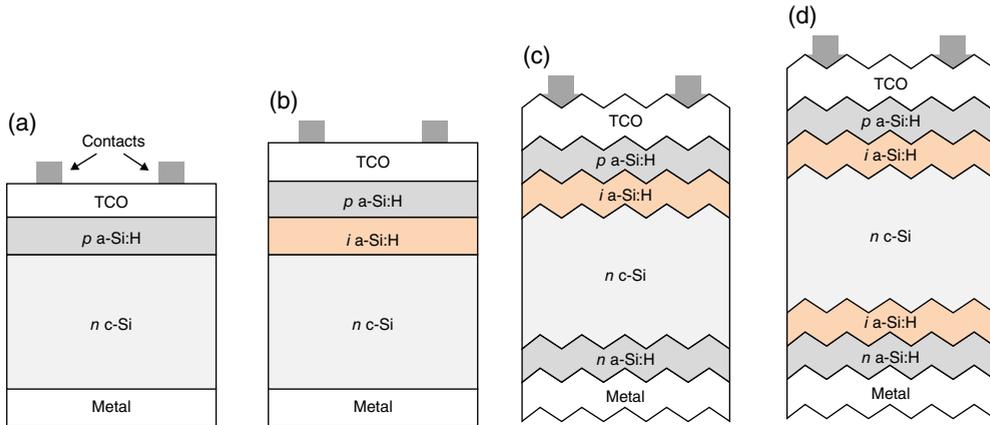
In practical heterojunction solar cells, such as the a-Si:H/c-Si one, the band offsets between different materials are accommodated in both the conduction band and the valence band. This results in barriers for carrier transport. Figure 3.4.2 shows the band diagram of *p*-type a-Si:H (bandgap 1.7 eV) and *n*-type c-Si (bandgap 1.1 eV). As indicated in Figure 3.4.2, the holes experience a spike which acts as a barrier to hole transport. Holes can move from c-Si to a-Si:H by tunnelling, trap-assisted tunnelling and/or thermionic emission (Zeman and Zhang, 2012).

Figure 3.4.3 shows the development of the structure of SHJ cells, illustrating increased complexity. The basic structure consists of a *p*-type a-Si:H layer on top of an *n*-type c-Si wafer. With this solar cell Sanyo achieved an efficiency of 12.3% (Tanaka *et al.*, 1992). It was shown that the optimal *p*-type a-Si:H layer thickness in terms of efficiency is 10 nm. It was found that a high defect-state density at the a-Si:H/c-Si interface is limiting the open-circuit voltage ( $V_{oc}$ ) and fill factor ( $FF$ ) of the device, i.e., 0.56 V and 0.71, respectively. The short-circuit current ( $J_{sc}$ ) was 30 mA/cm<sup>2</sup> at the maximum, and increasing the *p*-type a-Si:H layer thickness beyond 10 nm resulted in a decrease of  $J_{sc}$  due to absorption losses in the a-Si:H material.

To reduce the defect density at the *p*-*n* interface, a thin intrinsic a-Si:H layer between the *n*-type c-Si wafer and the *p*-type a-Si:H was introduced, which was denoted as ACJ-HIT (artificially constructed junction-heterojunction with intrinsic thin film) solar cell by Sanyo (Tanaka *et al.*, 1992). The thin intrinsic a-Si:H layer was to passivate the dangling bonds on the c-Si surface, and the a-Si:H/c-Si interface defect-state density was indeed reduced. This resulted in an improvement of  $V_{oc}$  and  $FF$  to 0.6 V and 0.79, respectively, with  $J_{sc}$  of 33 mA/cm<sup>2</sup>



**Figure 3.4.2** Energy band diagrams for (a) the separate materials *p*-type a-Si:H and *n*-type c-Si; and (b) the a-Si:H/c-Si heterojunction. Black and grey dots represent electrons and holes, respectively. The circle indicates the carrier (hole) transport through the energy barrier at the interface. Source: After Zeman and Zhang (2012)



**Figure 3.4.3** Schematic structure of heterojunction a-Si:H/c-Si solar cells. (a) basic structure with transparent conductive oxide and metal as top and back contact; (b) idem, with intrinsic a-Si:H layer sandwiched between p a-Si:H and n c-Si; (c) idem, with textured interfaces and back-surface field layer of n a-Si:H, (d) idem, with additional i a-Si:H. Note, drawings are not to scale

for an optimal intrinsic layer thickness of 4 nm. The highest efficiency was 14.8%. With increasing  $i$ -layer thickness, the absorption losses increase and as a consequence  $J_{sc}$  decreases. Also, the  $FF$  decreases due to the high resistivity of the intrinsic layer.

Further improvements have been achieved by introducing random texturing of the c-Si wafer to achieve optimal light trapping. At the same time, a back surface field (BSF) is introduced, which is formed by an  $n$ -type a-Si:H (Figure 3.4.3 (c)). The best device performance was  $J_{sc} = 37.9 \text{ mA/cm}^2$ ,  $V_{oc} = 0.614 \text{ V}$ ,  $FF = 0.78$ , and an efficiency of 18.6% (Tanaka *et al.*, 1992). A further step is to use intrinsic a-Si:H on both sides of the c-Si wafer for passivation. This yielded  $J_{sc} = 38.6 \text{ mA/cm}^2$ ,  $V_{oc} = 0.717 \text{ V}$ ,  $FF = 0.77$ , and efficiency of 21.3% (Tanaka *et al.*, 2003). In all device designs, transparent conductive oxides (TCOs) are necessary to facilitate carrier transport to the contacts as the a-Si:H are highly resistive. Usually, indium tin oxide (ITO) is used as the TCO.

The highest efficiency reported to date is 25.6%, using an interdigitated back contact structure to reduce the optical loss from absorption in the TCO layer and reflection by the front grid electrode. Silicon nitride was used as an antireflection layer, instead of the usual TCO layer. It was reported that the short-circuit current was improved to  $41.8 \text{ mA/cm}^2$ , and  $V_{oc} = 0.74 \text{ V}$ ,  $FF = 0.827$  (Masuko *et al.*, 2014).

### 3.4.3 Key Issues in a-Si:H/c-Si Cells

#### 3.4.3.1 Surface Passivation

Surface passivation of the c-Si wafer is a key requirement to optimize the performance of SHJ solar cells. The design of SHJ solar cells allows for the deposition of a surface passivating thin intrinsic layer consisting of a-Si:H before depositing the doped emitter and BSF layers, which can increase  $V_{oc}$ . The passivating properties of intrinsic a-Si:H have been widely studied

(Olibet *et al.*, 2007; Illiberi *et al.*, 2010; Schulze *et al.*, 2010; Schüttauf *et al.*, 2011), and excellent results have been obtained by various laboratories using different deposition techniques. For example, Schüttauf *et al.* (2011) compared different chemical vapor deposition (CVD) techniques, i.e., standard radio frequency plasma-enhanced CVD (rf-PECVD) at 13.56 MHz, very high frequency PECVD (VHF PECVD) at 50 MHz, and hot-wire CVD (HWCVD). It was shown that minority carrier lifetimes of 34–87  $\mu\text{s}$  could be obtained, which could be increased to values  $> 10$  ms after prolonged annealing at  $\sim 200^\circ\text{C}$ . Annealing is crucial as it enables the movement of hydrogen in the a-Si:H layer toward the a-Si:H/c-Si interface, which strongly reduces the dangling bond density at the interface (Olibet *et al.*, 2007; De Wolf *et al.*, 2012).

The excellent minority carrier lifetimes that can be obtained with a-Si:H can be explained by distinguishing different passivation mechanisms that govern the lifetime characteristics. Generally, surface passivation is ascribed to two different phenomena, namely, chemical passivation and field effect passivation. The former is caused by a reduction in defect states at the a-Si:H/c-Si interface, the latter by the repulsion of minority charge carriers from the interface by fixed charges. At high injection levels (light intensity) the Auger recombination also has to be taken into account (Schüttauf *et al.*, 2011). It was reported that the high quality of surface passivation, measured as surface recombination velocity (SRV), is mainly caused by a reduction in dangling bond density at the interface ( $N_{db}$ ) due to a saturation of dangling bonds by atomic hydrogen. The excellent c-Si surface passivation implies that the interface dangling bond density is on the order of  $10^8 \text{ cm}^{-2}$ . An SRV as low as 0.93 cm/s is calculated at an injection level of  $10^{15} \text{ cm}^{-3}$  (Schüttauf *et al.*, 2011).

In SHJ cells, the influence of the doped layers is also crucial (Schüttauf *et al.*, 2011; De Wolf *et al.*, 2012). The BSF creates additional field effect passivation, repelling minority charge carriers from the a-Si:H/c-Si interface at the back side, thereby further reducing recombination losses. On the emitter side, minority carriers are passing through the a-Si:H/c-Si interface region in the front side, which enhances the recombination losses. Furthermore, doped a-Si:H contains high levels of defect density, as the formation enthalpy for defects counteracting the active dopants is reduced when the Fermi level approaches one of the band edges (Street, 1991).

### 3.4.3.2 Wafer Cleaning

Before passivation layers are deposited, the c-Si wafer needs to be cleaned (Angermann *et al.*, 2009). Obviously, this is needed to remove any contamination present, but also the cleaning step in the processing sequence is used to partially passivate dangling bonds at the surface with hydrogen. One generally determines the quality of the cleaning step by measuring the carrier lifetimes using a Sinton contactless lifetime tester (Sinton and Cuevas, 1996). The RCA (Radio Corporation of America) cleaning method (Kern, 1970) is often used for high-lifetime processing of silicon wafers, which combines the removal of organic and inorganic metallic contaminants by a diluted solution of hydrogen peroxide with ammonia, followed by a diluted solution of hydrogen peroxide and hydrochloric acid, followed by an oxide removal step by hydrofluoric acid (HF) etching. This produces contamination-free c-Si surfaces that are temporarily chemically stable for further processing (Grundner and Jacob, 1986). Note that after cleaning, the wafers need to be transferred quickly to deposition systems to prevent fast native oxide growth on the c-Si surface.

### 3.4.3.3 Texturing

To lower material costs, c-Si wafers should be as thin as possible, however, this limits the absorption of light. This has prompted the development of textured surfaces as a means to increase light trapping. For c-Si wafers one generally uses a random pyramid texture. This can be attained using Si (100) substrates which are etched in alkaline solutions: the anisotropic etching yields Si (111) faceted pyramids (Bean, 1978), which lowers external reflection and at the same time improves internal reflection. Subsequent deposition of layers that are uniform in thickness is possible on the flat facets of the pyramids using CVD techniques.

### 3.4.4 Advantages Compared to c-Si Cells

In conventional c-Si solar cells, the p–n junction is formed by a thermal diffusion for which temperatures around 900 °C are required. In case of a-Si:H/c-Si-based heterojunction solar cell, processing, temperatures below 200 °C are typically used, as the p–n junction is formed by depositing a thin doped a-Si:H layer on a c-Si wafer (Van Sark *et al.*, 2012). This lower temperature processing (1) decreases the thermal budget of the production process; (2) limits the thermal degradation of the c-Si wafer quality; (3) enables the use of thinner wafers (<100 μm), avoiding warping issues associated with traditional high temperature processing; and (4) results in reduced environmental impact and production costs (Louwen *et al.*, 2015). Low-temperature (<200 °C) processing of a-Si:H/c-Si-based heterojunction solar cell is actually required after the a-Si:H film silicon deposition to avoid recrystallization by epitaxy of the amorphous film. This requirement, however, complicates the formation of low-resistivity metallized contacts for SHJ solar cells.

Light-induced degradation of performance that is usually seen in a-Si:H devices (Part 5) is not observed for a-Si:H/c-Si cells. This is due to the fact that the amorphous layers are very thin (5–10 nm) and their contribution to power generation can be ignored.

The temperature coefficient of a-Si:H/c-Si cells is lower than that of c-Si cells: the efficiency decreases as the function of the temperature is less severe for a-Si:H/c-Si cells. Although the a-Si:H layer is thin, its effect on the improvement of the surface passivation and as a consequence the higher  $V_{oc}$  has been shown to lead to this improved temperature dependence (Taguchi *et al.*, 2008). The lower temperature coefficient explains the higher annual yields for SHJ modules compared to conventional c-Si technology.

### List of Symbols

Symbol	Description	Unit
$\Delta E_c$	Conduction band discontinuity	eV
$E_{c1}$	Conduction band material 1	eV
$E_{c2}$	Conduction band material 2	eV
$\epsilon_1$	Permittivity of material 1	–
$\epsilon_2$	Permittivity of material 2	–
$E_F$	Fermi level	eV
$E_{F1}$	Fermi level of material 1	eV
$E_{F2}$	Fermi level of material 2	eV
$E_{g1}$	Bandgap material 1	eV

Symbol	Description	Unit
$E_{g2}$	Bandgap material 2	eV
$E_{vac}$	Vacuum energy level	eV
$FF$	Fill factor	–
$J_{sc}$	Short-circuit density	mA/cm <sup>2</sup>
$k$	Boltzmann constant ( $1.38064852 \times 10^{-23}$ )	m <sup>2</sup> kg s <sup>-2</sup> K <sup>-1</sup>
$n_i$	Intrinsic carrier density	cm <sup>-3</sup>
$N_{a2}$	Acceptor density of material 2	cm <sup>-3</sup>
$N_{c1}$	Effective density of states at the conduction band edge of material 1	cm <sup>-3</sup>
$N_{d1}$	Donor density of material 1	cm <sup>-3</sup>
$N_{DB}$	Dangling bond density at interface	cm <sup>-2</sup>
$N_{v2}$	Effective density of states at the valence band edge of material 2	cm <sup>-3</sup>
$q$	Elementary charge ( $1.60217662 \times 10^{-19}$ )	C
$\chi_1$	Electron affinity of material 1	V
$\chi_2$	Electron affinity of material 2	V
$\Phi_i$	Built-in voltage	V
$\Phi_{n1}$	Work function of material 1	V
$\Phi_{p2}$	Work function of material 2	V
$T$	Temperature	K
$V_{bi}$	Built-in voltage	V
$V_{oc}$	Open-circuit voltage	V

## List of Acronyms

Acronym	Meaning
ACJ-HIT	Artificially Constructed Junction-Heterojunction with Intrinsic Thin film
BSF	Back Surface Field
CVD	Chemical Vapor Deposition
CIGS	Copper Indium Gallium diSelenide
HF	Hydrofluoric acid
HIT	Heterojunction with Intrinsic Thin layer
HWCVD	Hot-Wire Chemical Vapor Deposition
ITO	Indium Tin Oxide
RCA	Radio Corporation of America
rf-PECVD	radio frequency Plasma-Enhanced Chemical Vapor Deposition
SHJ	Silicon HeteroJunction
SRV	Surface Recombination Velocity
TCO	Transparent Conductive Oxide
VHF	Very High Frequency

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